MachXO3D Development Board

Evaluation Board User Guide

FPGA-EB-02020-1.0

May 2020

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS and with all faults, and all risk associated with such information is entirely with Buyer. Buyer shall not rely on any data and performance specifications or parameters provided herein. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. No Lattice products should be used in conjunction with mission- or safety-critical or any other application in which the failure of Lattice's product could create a situation where personal injury, death, severe property or environmental damage may occur. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ASC	Analog Sense and Control
CMOS	Complementary Metal-Oxide Semiconductor
GDDR	Graphics Double Data Rate
FTDI	Future Technology Devices International
GPIO	General Purpose Input/Output
I^2C	Inter-Integrated Circuit
I3C	The MIPI I3C Sensor Interface, is an evolution of I^2C
LDO	Low Dropout
LVDS	Low-Voltage Differential Signaling
SPI	Serial Peripheral Interface

1. Introduction

The Lattice Semiconductor MachXO3D™ Development Board allows designers to investigate and experiment with the features of the MachXO3D device. The features of the MachXO3D Development Board can assist engineers with the rapid prototyping and testing of their specific designs.

The MachXO3D Development Board is part of the MachXO3D Development Kit, which includes the following:

- MachXO3D Development Board pre-loaded with the demo design
- Mini USB cable
- Quick Start Guide

This document is intended to be referenced in conjunction with MachXO3D demo user guides. See the References section.

The contents of this user guide include top-level functional descriptions of the various portions of the development board, descriptions of the onboard headers, diodes and switches, and a complete set of schematics.

1.1. MachXO3D Development Board

Along with the MachXO3D-9400HC device, the MachXO3D Development Board also includes features to expand the usability of the MachXO3D-9400HC with Arduino, Raspberry, FX12, Versa, and Aardvark headers.

Figure 1.1 shows the top view of the MachXO3D Development Board.

Figure 1.2 shows the bottom view of this board.

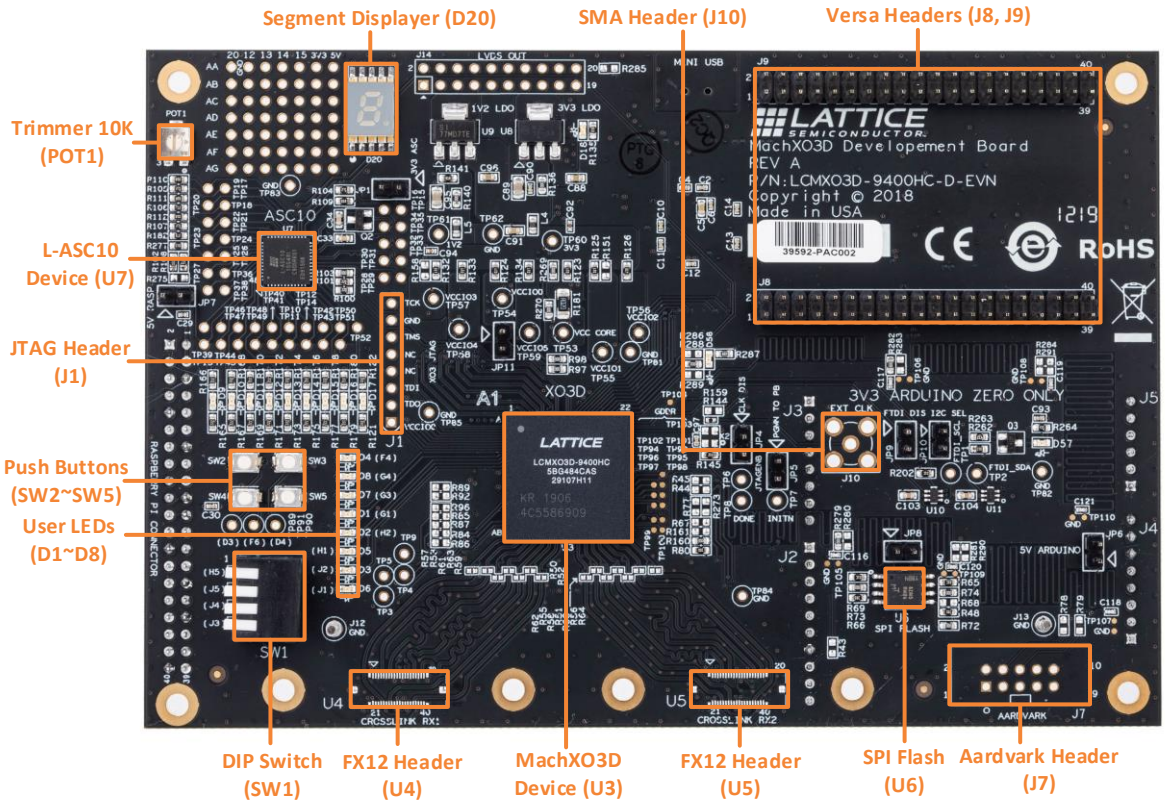

Figure 1.1. Top View of MachXO3D Development Board

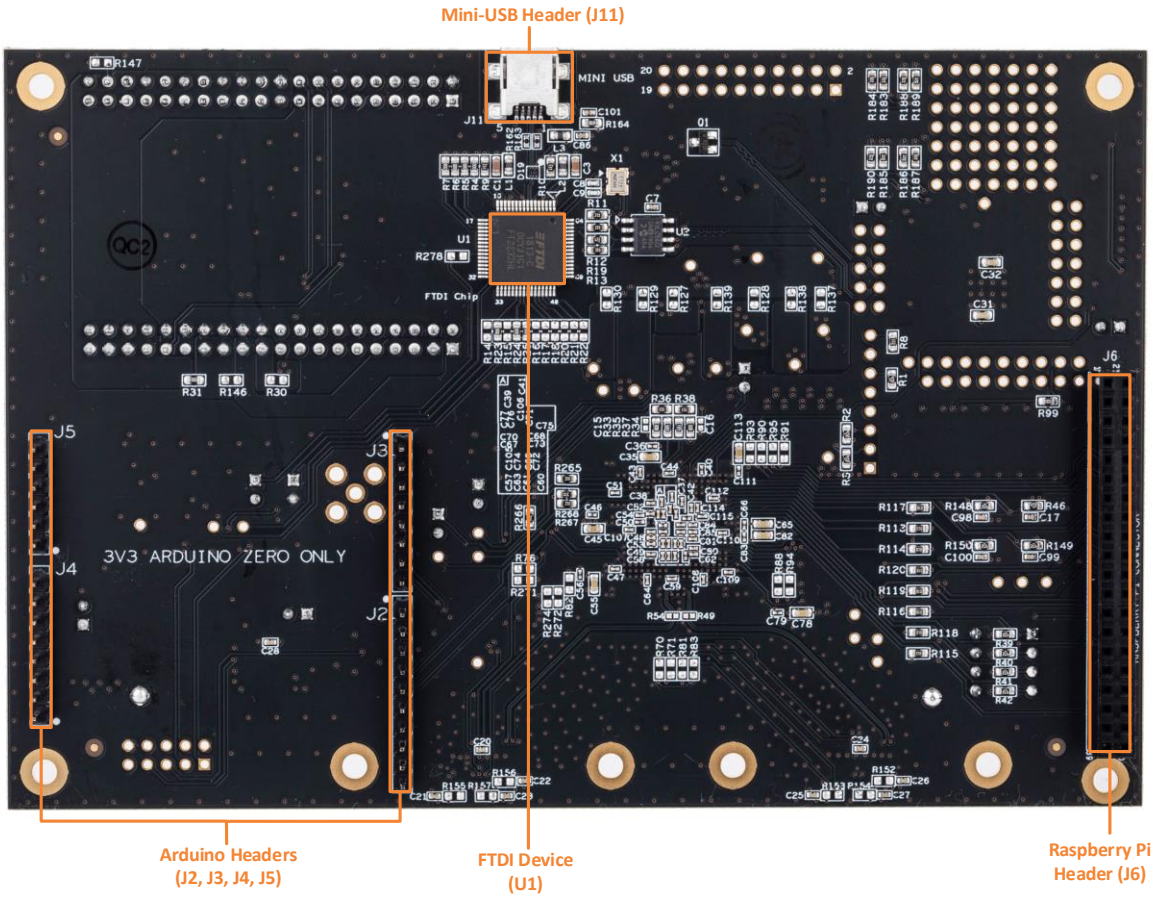

Figure 1.2. Bottom View of MachXO3D Development Board

1.2. Features

- LCMXO3D-9400HC demonstration
- General Purpose Input/Output (GPIO) interface with Arduino and Raspberry Pi boards
- USB-B connection for device programming and Inter-Integrated Circuit (I^2C) utility
- Onboard Boot Flash – 128 Mbit Serial Peripheral Interface (SPI) Flash with Quad read feature for user's application
- 7-Segment Blue LED, 4-position DIP Switches, 4 push buttons, and 16 red LEDs for demo purposes
- Lattice Diamond® programming support
- Multiple reference clock sources
- Two Hirose FX12-40 header positions (DNI)
- Aardvark header (DNI)

Note: DNI stands for "Do NOT Install" parts and DI stands for "Do Install" parts for assembly.

Caution: The MachXO3D Development Board contains ESD-sensitive components. ESD safe practices should be followed while handling and using the development board.

1.3. MachXO3D Device

The MachXO3D Development Board features the MachXO3D-9400HC in a 484-ball caBGA package. This device offers a variety of features and programmability that enhances Secure Control PLD functionality with hardware Root-of-Trust and Dual Boot capabilities. Its immutable Embedded Security Block offers cryptographic functions such as ECDSA256, SHA256, HMAC, ECIES, ECDH, AES-128/256, PUF, Public/Private Key Generation, and True Random Number Generator. Along with the Embedded Security Block, numerous system functions are included such as two PLLs and 432 kbits of embedded RAM plus hardened implementations of I^2C and SPI. Flexible, high performance I/O support numerous single-ended and differential standards including LVDS. For more information on the capabilities of MachXO3D, see MachXO3D Family Data Sheet (FPGA-DS-02026).

1.4. L-ASC10 Device

The L-ASC10 (also referred to as ASC, or Analog Sense and Control) is a Hardware Management (Power, Thermal, and Control Plane Management) Expander designed to be used with Platform Manager 2 or MachXO2™/MachXO3 FPGAs to implement the Hardware Management Control function in a circuit board. The L-ASC10 is included on this board for future expansion. This design flow is not supported in Diamond 3.11 SP2 or earlier. Check the Lattice website – www.latticesemi.com – for the latest news and support information for the MachXO3D + L-ASC10.

The L-ASC10 enables seamless scaling of power supply voltage and current monitoring, temperature monitoring, sequence and margin control channels. ASC includes dedicated interfaces supporting the exchange of monitor signal status and output control signals with centralized hardware management controllers. For more information on the capabilities of ASC device, see L-ASC10 In-System Programmable Hardware Management Expander Data Sheet (FPGA-DS-02038).

2. Applying Power to the Board

The MachXO3D Development Board is ready to power on with onboard Low Dropout (LDO) generators powered by an external 5 V power, as shown in Figure 2.1. The 5 V power can come from a USB connection (J11) and routed to multiple onboard headers listed in Table 2.1. Note that the 5 V power path to headers should be manually connected using a short resistor or jumper before power is applied to the mated board as outlined in Table 2.1.

Table 2.1. 5 V Sources and Connections

Header (Reference)	5 V Power Pins	5 V Power Path (Assembly)
USB header (J11)	1	L3 (DI)
FX12 header 1 (U4)	23, 38	R153 (DNI)
FX12 header 2 (U5)	23, 38	R155 (DNI)
Aardvark header (J7)	4, 6	R78 (DNI), R79 (DNI)
Arduino header (J4)	5	JP6 (DNI)
Raspberry Pi header (J6)	2, 4	JP7 (DNI)
Versa header (J8)	21	R30 (DNI)

Warning: Avoid power conflict when the 5 V power path is enabled from the MachXO3D Development Board to the mated board. Do Not apply 5V power from both boards when the path in the table is configured shorted.

Conversely, 5 V power can be supplied from onboard headers if J11 is not connected to a USB cable. The power from the headers can be used to drive LDOs and other mated boards.

Aside from the 3.3 V LDO (U8) default power source for MachXO3D device (U3), the board provides additional LDO footprint (U9) for lower power applications. SOT-223 footprint compatible LDOs from 1.2 V to 3.3 V can also be considered. Currently TLV1117LV12DCY is used to provide 1.2 V for optional VCCIOs. VCCIO1 for Bank 1, and VCCIO3 for Bank 3 can likewise be supplied from mated boards for better GPIO voltage alignment.

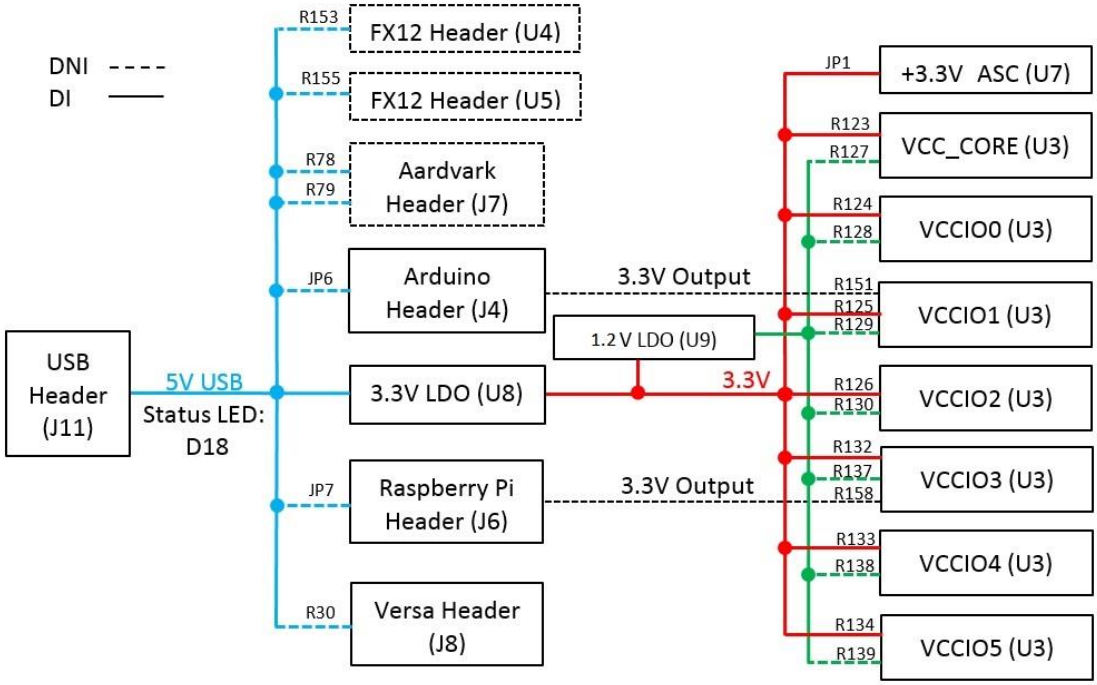

Figure 2.1. Board Power Supply

Table 2.2. MachXO3D Power Rail Options

MachXO3D Power (U3)	3.3 V Option (Assembly)	1.2V~3.3 V Option (Assembly)	Mated Board Option (Assembly)
VCC Core	R123 (DI)	R127 (DNI)*	NA
VCCIO0	R124 (DI)	R128 (DNI)	NA
VCCIO1	R125 (DI)	R129 (DNI)	R151 (DNI) for Arduino header
VCCIO2	R126 (DI)	R130 (DNI)	NA
VCCIO3	R132 (DI)	R137 (DNI)	R158 (DNI) for Raspberry Pi header
VCCIO4	R133 (DI)	R138 (DNI)	NA
VCCIO5	R134 (DI)	R139 (DNI)	NA

***Note:** R127 is applicable only in 2.5 V~3.3 V (U9) range for LCMXO3D-9400HC device.

Warning: Only one option should be enabled for each MachXO3D device power rail.

The ASC device (U7) acquires power from the 3.3 V LDO only. A jumper (JP1) needs to be installed to provide the power and this can also be used as test point to measure current drawn by the ASC.

Table 2.3. ASC Power Connections

ASC Power	ASC Power Pins	ASC Power Isolation (Assembly)
3.3 V VCC	8, 33 of U7	JP1 (DI)

3. JTAG/I²C Programming

The JTAG/I²C programming architecture of the MachXO3D Development Board is shown in Figure 3.1.

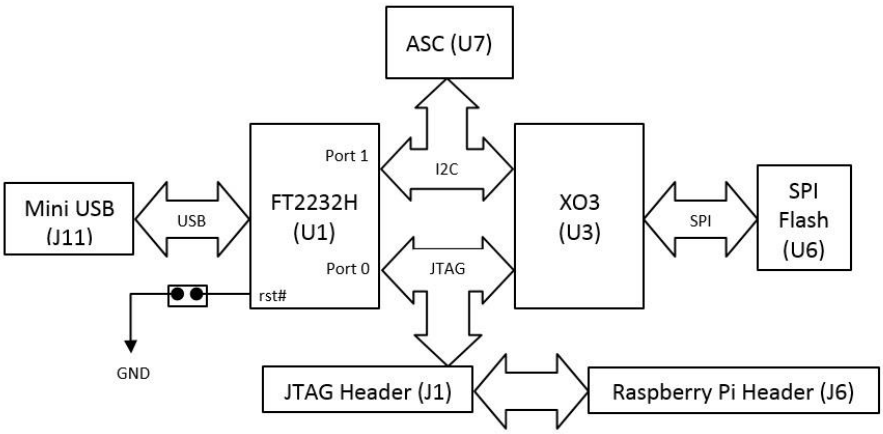

Figure 3.1. JTAG/I²C Programming Architecture

3.1. JTAG Download Interface

The MachXO3D Development Board has a built-in download controller for programming the MachXO3D device. It uses an FT2232H Future Technology Devices International (FTDI) part to convert USB to JTAG. To use the built-in download cable, connect the USB cable from J11 to your PC (with Diamond programming software installed). A mini USB to USB-A cable is included in the MarchXO3D Development Kit. The USB hub on the PC detects the cable of the USB function on Port 0, making the built-in cable available for use with the Diamond programming software. Using JTAG Programming for the Access mode is shown in Figure 3.2.

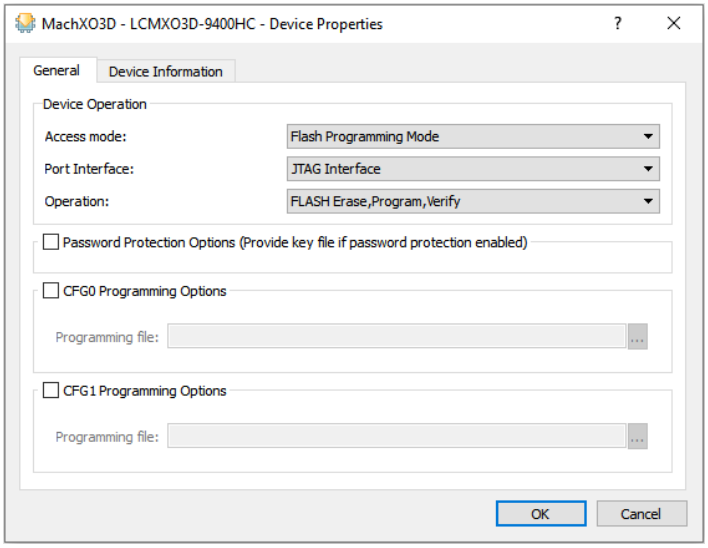

Figure 3.2. JTAG Programming Mode

3.2. I²C Download Interface

The USB hub on the PC can also detect the addition of the USB function on Port 1. Select the port FTUSB-1 on the programmer interface and enable the I²C MUX path from FTDI to the I²C bus. This is done by setting the J10 jumper (D57 red LED is lighted). The I²C interface programming can be also used to configure the MachXO3D device as shown in Figure 3.3, however, make sure that the I²C port is not disabled by the current working pattern.

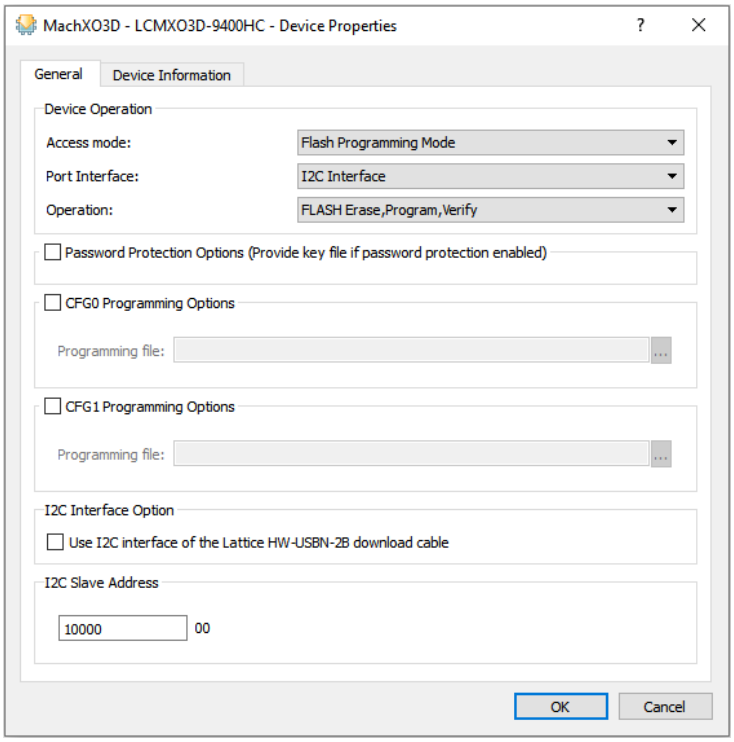

Figure 3.3. I²C Programming Mode

3.3. Alternate JTAG Download Interface

J1 is an 8-pin standalone JTAG header that is used with an external Lattice download cable (available separately) when the FTDI part is disabled from the JTAG chain after setting JP9. A USB download cable can be attached to the board using J1 to interface with the MachXO3D device. For details on the connection between the USB download cable and J1, refer to Programming Cable User Guide (FPGA-UG-02042).

J1 can also be used as test point when USB to JTAG is working. Additionally, you can enable the JTAG access path through the Raspberry Pi header (J6) for customer applications. This is done by connecting the J6 header to the J1 header through some onboard resistors. The JTAG connections between J1 and J6 are listed in Table 3.1.

Table 3.1. JTAG Connections

J1 Pin Number	JTAG Signal Name	MachXO3D Ball Location for JTAG	J6 Pin Number	J1 to J6 Isolation (Assembly)	Raspberry Pi GPIO
1	VCCIO0	—	—	—	—
2	TDO	E8	10	R90 (DNI)	IO15
3	TDI	E9	11	R93 (DNI)	IO17
4	—	—	—	—	—
5	—	—	—	—	—
6	TMS	C10	12	R91 (DNI)	IO18
7	GND	—	—	—	—
8	TCK	D10	8	R95 (DNI)	IO14

3.4. JTAG to MSPI Pass-through Interface

The download controller can also access the JTAG to MSPI pass-through circuit that allows the slave SPI Flash to be erased, programmed, and read with Diamond Programmer.

3.5. Other JTAG Configuration Pins

The MachXO3D Development Board provides test points for other JTAG configuration pins as shown in Table 3.2.

Table 3.2. Other JTAG Signals

Signal Name	MachXO3D Ball Location	Test Point
JTAGENB	E14	TP6
PROGRAMN	E15	Pin 1 of JP5
INITN	F16	TP7
DONE	E17	TP8

For more information on MachXO3D JTAG/ I^2C programming, refer to MachXO3D Programming and Configuration Usage Guide (FPGA-TN-02069).

4. MachXO3D Clock Sources

The MachXO3D Development Board has four options for the MachXO3D clock sources:

- 12 MHz from U1 (FTDI)
- 8 MHz from U7 (ASC)
- User defined frequency by installing an oscillator in the X2 (DNI) footprint
- Off-board clock source from J10 (DNI)

The 8 MHz clock from U7 is the default clock source when building a Platform Manager design. Note that JP1 should be installed to power the ASC device.

The 12 MHz clock from the FT2232H FTDI device is another clock source. Its use requires JP11 to be installed to connect the 12 MHz clock signal to the MachXO3D device I/O. JP9 should not be installed to enable U1.

Table 4.1. Input Clock Options

Clock Frequency	Signal Name	MachXO3D Ball Location	Clock Source	Comments
8 MHz	ASC_CLK	L1	U7	JP1 installed, test point TP14.
12 MHz	12MHz	B10	U1	JP11 installed, JP9 removed.
User defined	OSC_IN	D22	X2 (DNI)	JP4 removed and OSC_EN signal (MachXO3D ball L20) Logic 1.
User defined	OSC_IN	D22	J10 (DNI)	X2 not installed, or OSC_EN signal (MachXO3D ball L20) Logic 0, or JP4 installed.

Additional information on using optional clock sources:

- The board provides an optional clock input for the MachXO3D from either the Oscillator (X2) or the SMA header (J10), as shown in Figure 4.1. Neither of them is populated.
- X2 should be installed by the end user, and it should be a 2.5 mm × 2.0 mm 4-SMD package. This is compatible with the ASDMB serial of the Ultra Miniature Pure Silicon™ Clock Oscillator from Abracon LLC. JP4 can be used to disable X2 output by pulling down OSC_EN, which can also be controlled by the L20 pin of MachXO3D.
- J10 should be installed by the end user. A Complementary Metal-Oxide Semiconductor (CMOS) compatible clock can then be connected to an SMA cable.

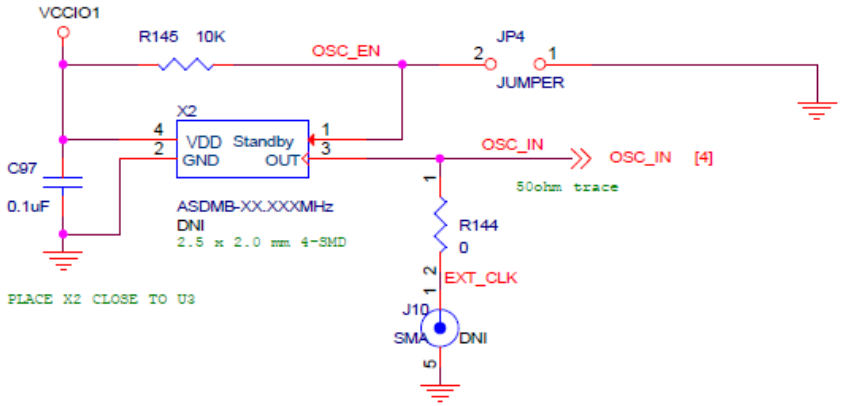

Figure 4.1. Optional Clock Circuit Design

5. Headers and Test Connections

This section describes the MachXO3D Development Board headers and test connections.

5.1. Versa Headers

The board provides two headers – J8 and J9 for expansion purpose.

Table 5.1. Versa J8 Header Pin Connections

J8 Pin Number	Signal Name	MachXO3D Ball Location
1	GND	—
2	NC	—
3	EXPCON_2V5*	—
4	EXPCON_IO29	E12
5	EXPCON_IO30	D14
6	EXPCON_IO31	C15
7	EXPCON_IO32	C17
8	EXPCON_IO33	D15
9	EXPCON_IO34	C18
10	EXPCON_IO35	D16
11	EXPCON_IO36	C19
12	EXPCON_IO37	D17
13	EXPCON_IO38	D18
14	EXPCON_IO39	C20
15	EXPCON_IO40	E16
16	EXPCON_IO41	E13
17	EXPCON_IO42	F13
18	EXPCON_IO43	F15
19	EXPCON_IO44	G15
20	EXPCON_IO45	G12
21	5VIN*	—
22	GND	—
23	EXPCON_2V5*	—
24	GND	—
25	VCCIO0	—
26	GND	—
27	VCCIO0	—
28	GND	—
29	EXPCON_OSC*	—
30	GND	—
31	EXPCON_CLKIN	A10
32	GND	—
33	EXPCON_CLKOUT	A21
34	GND	—
35	EXPCON_3V3**	—
36	GND	—
37	EXPCON_3V3**	—
38	GND	—
39	EXPCON_3V3**	—
40	GND	—

Notes:

* Signal is optionally connected to power source through resistor DNI.

** Signal is optionally connected to power source through resistor DI.

Table 5.2. Versa J9 Header Pin Connections

J9 Pin Number	Signal Name	MachXO3D Ball Location
1	HPE_RESOUT#	G9
2	GND	—
3	EXPCON_IO0	F8
4	EXPCON_IO1	G8
5	EXPCON_IO2	F9
6	EXPCON_IO3	F7
7	EXPCON_IO4	E7
8	EXPCON_IO5	E6
9	EXPCON_IO6	D5
10	EXPCON_IO7	C3
11	EXPCON_IO8	D6
12	EXPCON_IO9	C4
13	EXPCON_IO10	F10
14	EXPCON_IO11	C5
15	EXPCON_IO12	C6
16	EXPCON_IO13	B12
17	EXPCON_IO14	D7
18	EXPCON_IO15	A12
19	GND	—
20	EXPCON_3V3**	—
21	EXPCON_IO16	D8
22	GND	—
23	EXPCON_IO17	C8
24	GND	—
25	EXPCON_IO18	D9
26	GND	—
27	EXPCON_IO19	E10
28	EXPCON_IO20	C9
29	EXPCON_IO21	G11
30	GND	—
31	EXPCON_IO22	E11
32	EXPCON_IO23	D11
33	EXPCON_IO24	F11
34	GND	—
35	EXPCON_IO25	D12
36	EXPCON_IO26	F12
37	EXPCON_IO27	D13
38	CARDSEL#*	—
39	EXPCON_IO28	C14
40	GND	—

Notes:

* Signal is optionally connected to power source through resistor DNI.

** Signal is optionally connected to power source through resistor DI.

5.2. Arduino Board GPIO Headers

The board provides four headers, J2, J3, J4, and J5, for Arduino Zero board adaption.

Table 5.3. Arduino J2 Pin Connections

J2 Pin Number	Signal Name	Arduino ZERO Board Signal	MachXO3D Ball Location	Comments
1	AR_IO8	~8	U21	—
2	AR_IO9	~9	U22	—
3	AR_SS_IO10	~10	W20	Optional connection to SS through R67 for SPI access, DNI by default.
4	AR_MOSI_IO11	~11	V18	Optional connection to SISPI through R82 for SPI access, DNI by default.
5	AR_MISO_IO12	~12	G16	Optional connection to SPISO through R77 for SPI access, DNI by default.
6	AR_SCK_IO13	~13	F17	Optional connection to MCLK through R76 for SPI access, DNI by default.
7	GND	GND	—	—
8	AR_AREF	AREF	U17	AR_AREF connection to AREF through R43, DNI by default.
9	AR_SDA	SDA	U19	Optional connection to SDA0 through R44, DNI by default.
10	AR_SCL	SCL	U18	Optional connection to SCL0 through R45, DNI by default.

Table 5.4. Arduino J3 Pin Connections

J3 Pin Number	Signal Name	Arduino ZERO Board Signal	MachXO3D Ball Location
1	AR_IO0	RX <- 0	G19
2	AR_IO1	TX -> 1	G20
3	AR_IO2	2	G21
4	AR_IO3	~3	H20
5	AR_IO4	~4	G18
6	AR_IO5	~5	L21
7	AR_IO6	~6	W22
8	AR_IO7	7	V22
9	AR_SDA	SDA	U19
10	AR_SCL	SCL	U18

Table 5.5. Arduino J4 Pin Connections

J4 Pin Number	Signal Name	Arduino ZERO Board Signal	MachXO3D Ball Location	Comments
1	AR_IO14	ATN	T17	—
2	NC	IOREF	—	—
3	AR_RESET	RESET	U20	Pin U20 should be set high by default. Avoid Arduino ZERO board in Reset status when connected.
4	+3.3V_AR	3.3 V	—	3.3 V power supply from Arduino ZERO board.
5	AR_5V	5 V	—	Jump to 5 V main power through JP6.
6	GND	GND	—	—
7	GND	GND	—	—
8	+12V	VIN	—	12 V power supply from Arduino ZERO board.

Note: If JP6 is installed, 5 V power can be supplied from either the Arduino board or the MachXO3D Development Board. With JP6 removed, both boards need their own 5 V power

Table 5.6. Arduino J5 Pin Connections

J5 Pin Number	Signal Name	Arduino ZERO Board Signal	MachXO3D Ball Location	Comments
1	AR_AD0	A0	P19	Used as GPIO in digital mode.
2	AR_AD1	A1	P18	Used as GPIO in digital mode.
3	AR_AD2	A2	P17	Used as GPIO in digital mode.
4	AR_AD3	A3	P16	Used as GPIO in digital mode.
5	AR_AD4	A4	K22	Used as GPIO in digital mode.
6	AR_AD5	A5	G17	Used as GPIO in digital mode.

5.3. FX12 Headers (DNI)

The board provides two headers, U4 and U5, to connect to FX12 compatible boards or cables. Each header has eight pairs of Low-Voltage Differential Signaling (LVDS) signals for high-speed data receiver.

Table 5.7. FX12 U4 Header Pin Connections

U4 Pin Number	Signal Name	MachXO3D Ball Location
1	CH0_DCK_P	AA10
2	CH0_DCK_N	AB10
3	GND	—
4	CH0_DATA0_P	AA4
5	CH0_DATA0_N	AB4
6	GND	—
7	CH0_DATA2_P	AA5
8	CH0_DATA2_N	AB5
9	GND	—
10	FX_SN*	—
11	FX_SCLK*	—
12	PWR_12V**	—
13	SDA2	AB13
14	SCL2	AA13
15	GND	—
16	CH2_DATA0_P	AA6
17	CH2_DATA0_N	AB6
18	GND	—
19	CH2_DCK_P	AA7
20	CH2_DCK_N	AB7
21	PWR_12V**	—
22	RESETN	AB3
23	PWR_5-0V*	—
24	CH0_DATA1_P	AA2
25	CH0_DATA1_N	AB2
26	PWR_3-3V*	—
27	CH0_DATA3_P	AA8
28	CH0_DATA3_N	AB8
29	PWR_1-8V*	—
30	FX_MOSI*	—

U4 Pin Number	Signal Name	MachXO3D Ball Location
31	FX_MISO*	—
32	PWR_1-8V*	—
33	GND	—
34	GND	—
35	PWR_3-3V*	—
36	CH2_DATA1_P	AA9
37	CH2_DATA1_N	AB9
38	PWR_5-0V*	—
39	SDA1	AA11
40	SCL1	AB11

Notes:

* Signal is optionally connected to power source through resistor DNI.

** 12 V power needs external supply from pin 8 of J4.

Table 5.8. FX12 U5 Header Pin Connections

U5 Pin Number	Signal Name	MachXO3D Ball Location
1	CH1_DCK_P	AB12
2	CH1_DCK_N	AA12
3	GND	—
4	CH1_DATA0_P	AB16
5	CH1_DATA0_N	AA16
6	GND	-
7	CH1_DATA2_P	AB17
8	CH1_DATA2_N	AA17
9	GND	—
10	FX_SN*	—
11	FX_SCLK*	—
12	PWR_12V**	—
13	SDA2	AB13
14	SCL2	AA13
15	GND	—
16	CH3_DATA0_P	AB18
17	CH3_DATA0_N	AA18
18	GND	—
19	CH3_DCK_P	AB19
20	CH3_DCK_N	AA19
21	PWR_12V**	—
22	RESETN	AB3
23	PWR_5-0V*	—
24	CH1_DATA1_P	AB14
25	CH1_DATA1_N	AA14
26	PWR_3-3V*	—
27	CH1_DATA3_P	AB15
28	CH1_DATA3_N	AA15
29	PWR_1-8V	—
30	FX_MOSI*	—
31	FX_MISO*	—
32	PWR_1-8V*	—
33	GND	—

U5 Pin Number	Signal Name	MachXO3D Ball Location
34	GND	—
35	PWR_3-3V*	—
36	CH3_DATA1_P	AB20
37	CH3_DATA1_N	AA20
38	PWR_5-0V*	—
39	SDA1	AA11
40	SCL1	AB11

Notes:

* Signal is optionally connected to power source through resistor DNI.

** 12 V power needs external supply from pin 8 of J4.

5.4. Aardvark Header (DNI)

The Aardvark I^2C /SPI Host Adapter is a fast and powerful I^2C bus and SPI bus host adapter through USB. It allows you to interface a Windows, Linux, or Mac OS X PC through USB to a downstream embedded system environment and transfer serial messages using the I^2C and SPI protocols.

The MachXO3D Development Board provides an Aardvark compatible header for customer applications. The I^2C bus is capable of connecting to a global I^2C bus on the board, if JP10 is NOT set.

Table 5.9. Aardvark J7 Header Pin Connections

J7 Pin Number	Signal Name	MachXO3D Ball Location
1	J7_SCL	To I^2C analog switch U10
2	—	GND
3	J7_SDA	To I^2C analog switch U11
4	+5V_I2C	To VBUS_5V through R78, DNI
5	SPISO	To MachXO3D U9
6	+5V_SPI	To VBUS_5V through R79, DNI
7	MCLK	To MachXO3D T9
8	SISPI	To MachXO3D AA21
9	SS	Multiple options, as shown in Figure 5.1.
10	—	—

Caution: VCCIO2 should be 3.3 V when connected to Aardvark I^2C/SPI Host Adapter.

Pin 9 of the Aardvark header is an SS signal that can be optionally connected to multiple devices or connectors. By default, Pin 9 can access Slave SPI in the MachXO3D device as the Master SPI through R160. It can access FX12 header, Raspberry Pi header and on-board SPI Flash by enabling R161. It can also access the Arduino header by enabling R67.

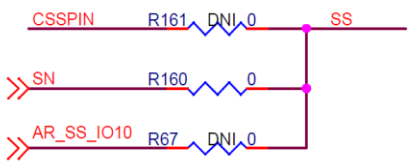

Figure 5.1. Aardvark SS Pin Connections

5.5. Raspberry Pi Board GPIO Header

The MachXO3D Development Board provides a 40-pin receptacle that is compatible with the GPIO header of Raspberry Pi 2/3 serial models.

Table 5.10. Raspberry Pi J6 Header Pin Connections

J6 Pin Number	Signal Name	MachXO3D Ball Location
1	3.3V_RASP*	—
2	RASP_5V**	—
3	RASP_IO02	U2
4	RASP_5V**	—
5	RASP_IO03	V1
6	GND	—
7	RASP_IO04	T6
8	RASP_IO14	P4
9	GND	—
10	RASP_IO15	N5
11	RASP_IO17	N6
12	RASP_IO18	N7
13	RASP_IO27	P5
14	GND	—
15	RASP_IO22	P6
16	RASP_IO23	R3
17	3.3V_RASP*	—
18	RASP_IO24	R4
19	RASP_IO10	R6
20	GND	—
21	RASP_IO09	R7
22	RASP_IO25	R5
23	RASP_IO11	T3
24	RASP_IO08	T4
25	GND	—
26	RASP_IO07	T5
27	RASP_ID_SD	V5
28	RASP_ID_SC	T7
29	RASP_IO05	U3
30	GND	—
31	RASP_IO06	U4
32	RASP_IO12	V4
33	RASP_IO13	U5
34	GND	—
35	RASP_IO19	W3
36	RASP_IO16	W4
37	RASP_IO26	P7
38	RASP_IO20	Y2
39	GND	—
40	RASP_IO21	Y3

Notes:

* 3.3 V power is supplied from Raspberry Pi board.

** 5 V power can come from either the Raspberry Pi board or the MachXO3D Development Board when jumper JP7 is installed. When jumper JP7 is not installed, both boards need their own 5 V power.

5.6. Dedicated I3C Test Points

The MachXO3D device features four pairs of I/O with I3C dynamic pull up capability in Bank 3. The MachXO3D Development Board routes out two pairs of unoccupied I/O to test points for customer applications.

Table 5.11. I3C Test Points

Test Points	Signal Name	MachXO3D Ball Location
TP3	I3C_AA1	AA1
TP4	I3C_Y1	Y1
TP5	I3C_U1	U1
TP9	I3C_T2	T2

5.7. Dedicated Slew Rate Test Circuits

MachXO3D device features two sets of test circuits to simulate the trace conditions for different board sizes, providing variable traces with 4-inch, 8-inch and 16-inch length for customer flexibility. Figure 5.2 shows one of the test circuits. The test conditions for different trace length are summarized in Table 5.12.

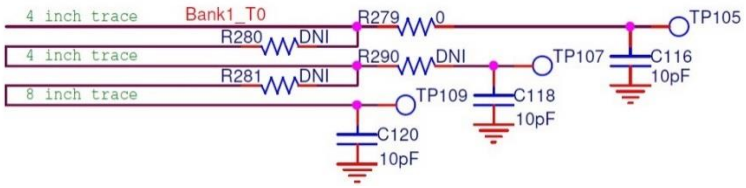

Figure 5.2

Figure 5.2. Slew Rate Test Circuits

Table 5.12. Slew Rate Test Conditions

MachXO3D Ball Location	IO Bank	Enable 4- inch Trace			Enable 8-inch Trace			Enable 16-inch Trace		
		Test Point	Load Cap	Path Config	Test Point	Load Cap	Path Config	Test Point	Load Cap	Path Config
M22	1	TP105	C116	R279(DI)	TP107	C118	R279(DNI)	TP109	C120	R279(DNI)
				R280(DNI)			R280(DI)			R280(DI)
				R290(DNI)			R290(DI)			R290(DNI)
				R281(DNI)			R281(DNI)			R281(DI)
B21	0	TP106	C117	R282(DI)	TP108	C119	R282(DNI)	TP110	C121	R282(DNI)
				R283(DNI)			R283(DI)			R283(DI)
				R291(DNI)			R291(DI)			R291(DNI)
				R284(DNI)			R284(DNI)			R284(DI)

6. I²C and SPI Buses

This section describes the MachXO3D Development Board I²C and SPI topology.

6.1. I²C Topology

The MachXO3D Development Board has a flexible I²C bus to support all optional connectors and devices on the board. The global I²C bus has the signal names SDA0 and SCL0, and they are routed close to the devices and headers as shown in Figure 6.1.

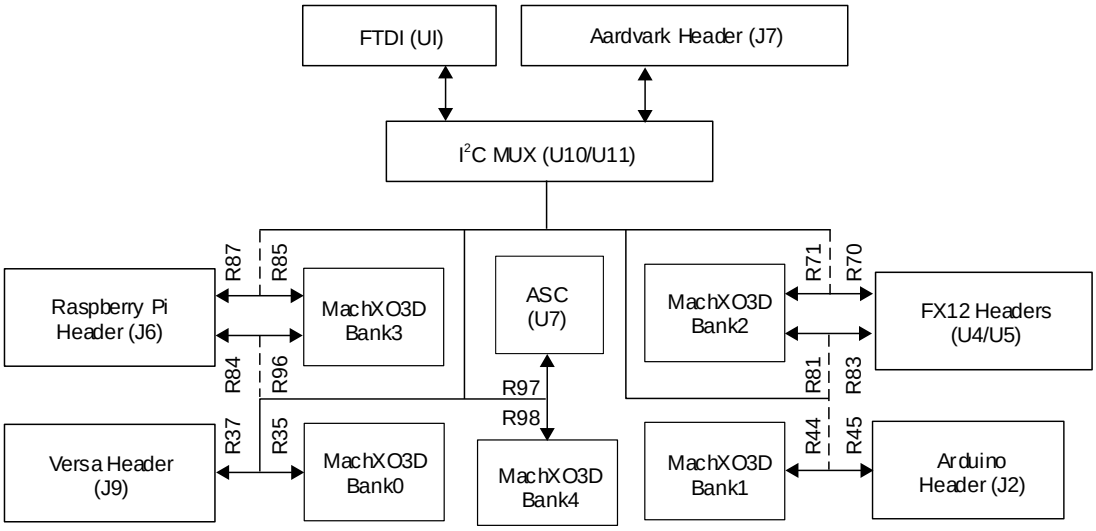

Figure 6.1. I²C Topology

The board provides two options for accessing the global I²C bus from external cables. One is from the mini USB cable (J11) through FTDI (U1). The other is from the Aardvark header (J7) for an Aardvark cable. Two analog MUXes, as shown in Figure 6.2, are used to select between the USB and Aardvark cables. Both MUXes are controlled by the signal USB_I2C_EN.

Table 6.1. I²C MUX Function

Global I²C Controller	USB_I2C_EN Logic Level	FSA4157 MUX Function	SCL0 Test Point	SDA0 Test Point
Aardvark Header (J7)	0 (JP10 removed)	J7_SCL <> SCL0 J7_SDA <> SDA0	Pin1 of J7	Pin3 of J7
USB FTDI (U1)	1 (JP10 installed)	FTDI_SCL <> SCL0 FTDI_SDA <> SDA0	TP1	TP2

When the jumper JP10 is removed, the USB_I2C_EN signal is low and the Aardvark header J7 is connected to the global I²C bus. When the jumper JP10 is installed, the USB_I2C_EN signal is high and the USB connector J11 is connected to the global I²C bus through the FTDI device.

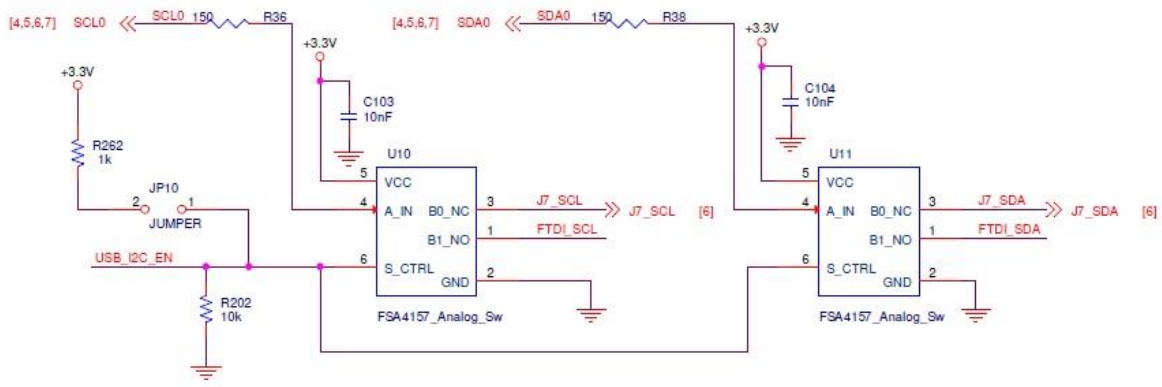

Figure 6.2. I²C MUX Circuits

To support a wide variety of I²C applications, each header or device is connected to a dedicated MachXO3D GPIO bank with a direct local I²C bus. Each local I²C bus can optionally connect to the global I²C bus through resistors. The local I²C connections are summarized in Table 6.2.

Table 6.2. I²C Global Bus Connections

MachXO3D Bank	Component (Reference)	Header Pin	MachXO3D Ball	Logical Signal Name (Global I²C Signal)	Resistor
0	Versa header (J9)	18	A12	EXPCON_IO15 (SDA0)	R37 (DI)*
		16	B12	EXPCON_IO13 (SCL0)	R35 (DI)*
1	Arduino header (J2)	9	U19	AR_SDA (SDA0)	R44 (DNI)
		10	U18	AR_SCL (SCL0)	R45 (DNI)
2	FX12 headers (U4/U5)	39	AA11	SDA1 (SDA0)	R81 (DNI)
		40	AB11	SCL1 (SCL0)	R83 (DNI)
		13	AB13	SDA2 (SDA0)	R71 (DNI)
		14	AA13	SCL2 (SCL0)	R70 (DNI)
3	Raspberry Pi header (J6)	3	U2	RASP_IO02 (SDA0)	R84 (DNI)
		5	V1	RASP_IO03 (SCL0)	R96 (DNI)
		27	V5	RASP_ID_SD (SDA0)	R87 (DNI)
		28	T7	RASP_ID_SC (SCL0)	R85 (DNI)
4	ASC device (U7)	14	K2	I2C_SDA0 (SDA0)	R97 (DI)*
		15	K1	I2C_SCL0 (SDA0)	R98 (DI)*

***Note**: The resistor needs to be installed to support programming of the ASC device. Versa header J9 pins 16 and 18 need to be high-Z to support programming of the ASC device. Balls B12 and A12 should be used in Platform Manager design. Balls K1 and K2 provide a connection for a user-instantiated I²C port as part of a separate system to communicate with the ASC device.

6.2. SPI Topology

6.2.1. SPI Configuration

One of the major functions of SPI connections on the board is to support MachXO3D configuration from SPI ports. The MachXO3D Development Board can support both Master SPI (MSPI) and Slave SPI (SSPI) modes for MachXO3D configuration.

Table 6.3. MachXO3D SPI Connections

Signal Name	MachXO3D Ball Location	MSPI Mode Direction	SSPI Mode Direction
MCLK	T9	Output	Input
SN	AB21	Input	Input
SISPI	AA21	Output	Input
SPISO	U9	Input	Output
CSSPIN	AA3	Output	Not used

The MachXO3D device can be configured from different ports on the board as listed in Table 6.4. By default, the MachXO3D device can boot up from SPI Flash with Master SPI mode.

Table 6.4. MachXO3D SPI Configuration Options

Master SPI Device (Reference)	Master CS (Pin Number of Reference Part)	Slave SPI Device (Reference)	Slave CS (Pin Number of Reference Part)
MachXO3D (U3)	CSSPIN (AA3)	SPI Flash (U6)	CS# (1)
MachXO3D (U3)	CSSPIN (AA3)	FX12 (U4, U5)	FX_SN (10)
Aardvark (J7)	SS (9)	MachXO3D (U3)	SN (AB21)
Arduino (J2)	AR_SS_IO10 (3)	MachXO3D (U3)	SN (AB21)
Raspberry Pi (J6)	Rasp_IO08 (24)	MachXO3D (U3)	SN (AB21)

For detailed information on Master SPI and Slave SPI mode configuration, refer to MachXO3D Programming and Configuration Usage Guide (FPGA-TN-02069).

6.2.2. SPI Flash Access

Onboard SPI Flash memory can be used to store the MachXO3D configuration data in either External or Dual Boot mode. It can also store customer data in certain applications. The MachXO3D device includes the JTAG to MSPI pass-through circuit that allows the slave SPI Flash to be erased, programmed, and read with Diamond Programmer. For detailed information on JTAG to MSPI pass-through for slave SPI Flash access, refer to MachXO3D Programming and Configuration Usage Guide (FPGA-TN-02069).

7. LEDs and Switches

LEDs and switches of the MachXO3D Development Board that can be used in demo and customer designs are described in this section.

7.1. Four-Position DIP Switch

Four MachXO3D pins are connected to the four switches of SW1, as shown in the circuit design in Figure 7.1. The CTS side actuated DIP switches are connected to logic level 0 when in the ON position, as shown in Figure 7.2.

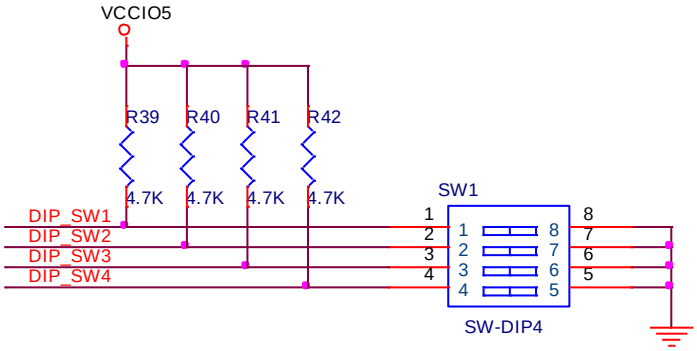

Figure 7.1. Four-Position DIP Switch Circuits

Figure 7.2. Four-Position DIP Switch Photograph

One side of each switch is connected to GPIOs within the VCCIO5 bank and pulled up through 4.7 kΩ resistors. The other side is grounded. The designated pins are connected, as shown in Table 7.1.

Table 7.1. Four-Position DIP Switch Signals

Signal Name	MachXO3D Ball Location	SW1 DIP Switch Position	4.7 kΩ Pull up Resistor	Logic Level at ON Position
DIP_SW1	H5	1	R39	0
DIP_SW2	J5	2	R40	0
DIP_SW3	J4	3	R41	0
DIP_SW4	J3	4	R42	0

7.2. General Purpose Push Buttons

The MachXO3D Development Board provides four push button switches, SW2, SW3, SW4, and SW5, for demos and user applications. Pressing these buttons drives a logic level *0* to the corresponding I/O pins.

Table 7.2. Push Button Switch Signals

Signal Name	MachXO3D Ball Location	Push Button Reference	Logic Level at Button Pressed
PB1	D3	SW2	0
PB2	D4	SW3	0
PB3	F6	SW4	0
PB4	G7	SW5	0

SW2, SW3, and SW4 are designed for general-purpose applications. SW5 is designed with additional jumper JP5, as shown in Figure 7.3. SW5 can be used as PROGRAMN push button when JP5 is set to trigger the configuration process without power cycle. For detailed information on PROGRAMN, refer to MachXO3D Programming and Configuration Usage Guide (FPGA-TN-02069).

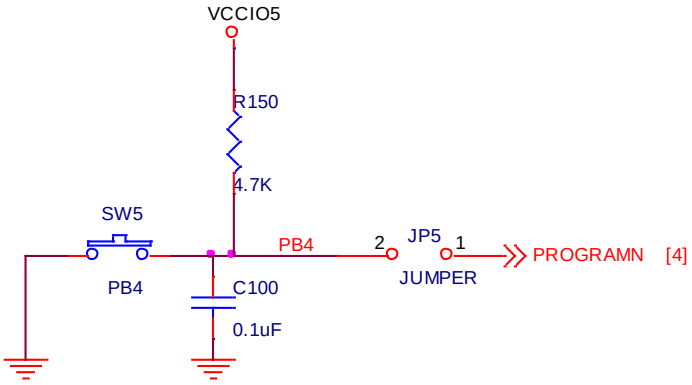

Figure 7.3. Push Button SW5 Circuit Design

7.3. General Purpose LEDs

The MachXO3D Development Board provides eight red LEDs that are connected to I/O within Bank 5. The LEDs are lighted when the output is driven LOW. Table 7.3 lists the red LEDs and their associated pins.

Table 7.3. LED Signals

Red LEDs	Signal Name	MachXO3D Ball Location	Logic Level to Light
D1	XLED0	G1	0
D2	XLED1	H2	0
D3	XLED2	J2	0
D4	XLED3	F4	0
D5	XLED4	H1	0
D6	XLED5	J1	0
D7	XLED6	G3	0

Note: The LEDs are not lined up in sequence, as shown in Figure 7.4.

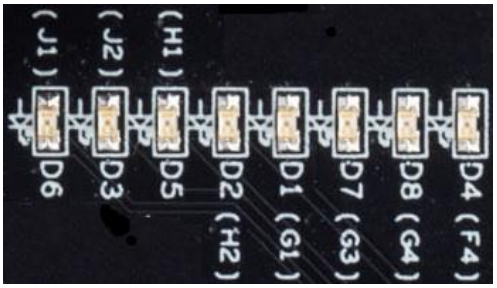

Figure 7.4. Board LEDs

7.4. LVDS Outputs Pins

The MachXO3D Development Board provides nine pairs of unused LVDS outputs pins that are connected to J14 for possible customer applications. The LVDS test points are detailed in Table 7.4.

Table 7.4. LVDS Test Points

Signal Name	MachXO3D Ball Location	Test Pin of J14	Comments
LVDS_OUT0_P	B1	1	LVDS output pair 0
LVDS_OUT0_N	A2	2	
LVDS_OUT1_P	B2	3	LVDS output pair 1
LVDS_OUT1_N	A3	4	
LVDS_OUT2_P	B3	5	LVDS output pair 2
LVDS_OUT2_N	A4	6	
LVDS_OUT3_P	B4	7	LVDS output pair 3
LVDS_OUT3_N	A5	8	
LVDS_OUT4_P	B5	9	LVDS output pair 4
LVDS_OUT4_N	A6	10	
LVDS_OUT5_P	B6	11	LVDS output pair 5
LVDS_OUT5_N	A7	12	
LVDS_OUT6_P	B8	13	LVDS output pair 6
LVDS_OUT6_N	A8	14	
LVDS_OUT7_P	B9	15	LVDS output pair 7
LVDS_OUT7_N	A9	16	
LVDS_OUT8_P	B11	17	LVDS output pair 8
LVDS_OUT8_N	A11	18	
GND	—	19	For test convenience
VCCIO0	—	20	For test convenience through R285 (DNI)

7.5. General Purpose DDR Outputs

Graphics Double Data Rate (GDDR) signals are wired to the test pads for signal validation.

Table 7.5. GDDR Test Points

Signal Name	MachXO3D Ball Location	Test Point
GDDR_DQ0	R22	TP93
GDDR_DQ1	R21	TP94
GDDR_DQ2	T22	TP95
GDDR_DQ3	T21	TP96
GDDR_DQ4	Y22	TP97
GDDR_DQ5	W21	TP98
GDDR_DQ6	AA22	TP99
GDDR_DQ7	Y21	TP100
GDDR_DQS	N22	TP101
GDDR_DQSN	P21	TP102

7.6. Seven-Segment Display

The MachXO3D Development Board features a blue Seven-Segment Display of D20, as shown in Figure 7.5, controlled by I/O within Bank 5. Each segment LED is lighted blue when the output is driven LOW. Table 7.6 lists the connections between display LED segments and their associated driver pins.

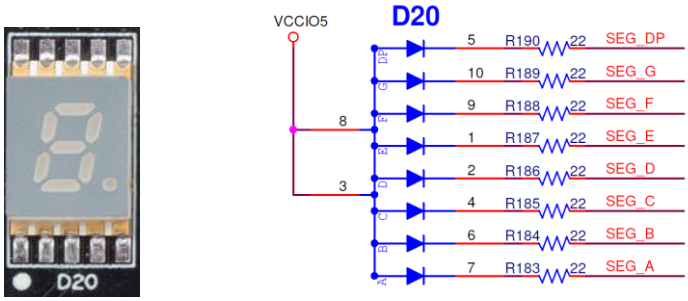

Figure 7.5. Seven-Segment Display and its Symbol

Table 7.6. Seven-Segment Display Connections

Signal Name	D20 Pin Number	MachXO3D Ball Location	Logic Level to Light
SEG_A	7	G2	0
SEG_B	6	D1	0
SEG_C	4	C1	0
SEG_D	2	D2	0
SEG_E	1	E2	0
SEG_F	9	E3	0
SEG_G	10	E1	0
SEG_DP	5	F1	0

8. ASC Connections

8.1. ASC Interface

Important: The MachXO3D + ASC design flow is NOT supported by Diamond 3.11 SP2 or earlier version. Check the Lattice website (www.latticesemi.com) for the latest news on MachXO3D + ASC design support. The ASC device is included on this board in anticipation of future support. The information provided below throughout this ASC section is for reference only.

The MachXO3D Development Board includes a dedicated ASC Interface (ASC-I/F) between the onboard ASC device and the MachXO3D Bank 4.

Table 8.1. ASC to MachXO3D Connections

ASC Connections	MachXO3D Ball Location	ASC Pins	Description	ASC Breakout Test Point
I2C_SDA0	K2	14	I^2C data programming (user control)	TP2
I2C_SCL0	K1	15	I^2C clock programming (user control)	TP1
ASC_ CLK	L1	7	8 MHz clock output from ASC	TP14
ASC_RESETb	L3	43	ASC device reset (Active Low)	TP13
ASC_WRCLK	M1	6	ASC-I/F clock signal to ASC	TP12
ASC_RDAT	N1	5	ASC-I/F data signal from ASC	TP11
ASC_WDAT	P1	4	ASC-I/F data signal to ASC	TP10
I2C_WRITE_PROTECT	N2	44	I^2C Configuration Write Control signal when WP[1:0] = 10 in ASC WRITEPROTECT_USERTAG Register; pull high to enable overwriting by I^2C instructions.	Share with TP44 for ASC_LED1 if R99 is installed.

8.2. ASC Voltage Monitor

ASC Voltage Monitors (VMONs) are connected to various power sources on the board, as listed in Table 8.2.

Table 8.2. ASC VMON Connections

Power Name	ASC Signal Name	ASC Pin Number	ASC Breakout Test Point
+2.5V**	ASC_VMON1	26	TP15
GND*	ASC_GS_VMON1	25	TP16
VCC1_8FT**	ASC_VMON2	28	TP17
GND*	ASC_GS_VMON2	27	TP19
+3.3V_RASP**	ASC_VMON3	30	TP18
GND*	ASC_GS_VMON3	29	TP20
+3.3V_AR**	ASC_VMON4	32	TP21
GND*	ASC_GS_VMON4	31	TP22
VBUS_5V**	ASC_VMON5	34	TP23
—	ASC_VMON6	35	TP24
POT***	ASC_VMON7	36	TP25
—	ASC_VMON8	37	TP26
+3.3V_ASC**	ASC_VMON9	38	TP27

Notes:

* Connection to GND is through 100 Ω (R109 – R112) so that the test point is not overdriven.

** Connection to the supply is through 270 Ω (R104 – R108, R182) so that the test point is not overdriven.

*** Connection to POT is through 1 kΩ (R277) so that the test point is not overdriven.

A 10 kΩ Trimmer Potentiometers (POT1) is used to provide voltage variation from 0 V - 3.3 V to ASC VMON7, as shown in Figure 8.1.

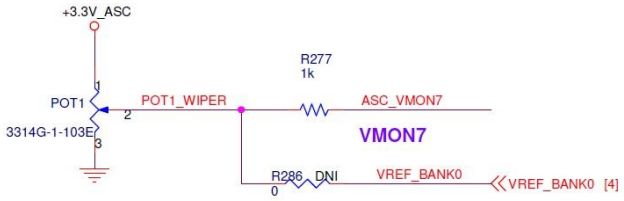

Figure 8.1. Trimmer Circuit Design for VMON7

Rotate the Trimmer clockwise to decrease the voltage, as shown in Figure 8.2, and to increase the voltage to VMON7, rotate the POT counter-clockwise.

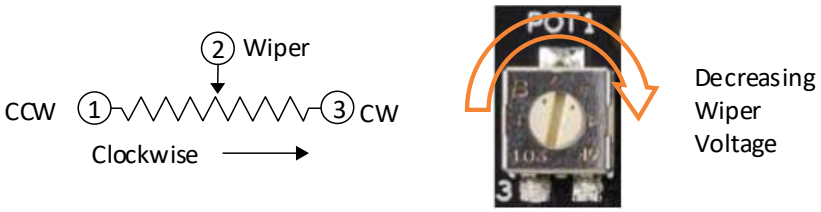

Figure 8.2. Trimmer Wiper Description

The Trimmer wiper can optionally be connected to a GPIO of MachXO3D Bank 0, providing the capability to evaluate the sysI/O features including LVCMOS25R33, LVCMOS18R33, LVCMOS15R33, LVCMOS12R33, LVCOMS10R33, and LVCMOS18R25 when VCCIO0=3.3V, as well as VCMOS15R25, LVCMOS12R25 and LVCMOS10R25 when VCCIO0=2.5V. For the Trimmer wiper voltage settings in detail to supply VREF, see MachXO3D Family Data Sheet (FPGA-DS-02026).

8.3. ASC Current Monitor

One of the ASC Current Monitors (IMONs) is connected to monitor the MachXO3D core current using resistor R181 as a shunt. The IMON uses the differential voltage across R181 to monitor the current. The ASC has two IMONs: one is used for lower voltage (–0.3 V to 5.9 V) current monitoring (pins 19 and 20), and the other HIMON (pins 17 and 18) is used for higher voltage (4.5 V to 13.2 V) current monitoring. Pin 18 is a shared input pin used for both HIMON and HVMON.

Table 8.3. ASC IMON Connections

Power Name	ASC Signal Name	ASC Pin Number	ASC Breakout Test Point	Comments
VCC_CORE	ASC_IMONP	19	TP30	R181 (0.020 Ω) is placed between P/N node for current measurement
	ASC_IMONN	20	TP31	
User Connected	ASC_HIMONP	17	TP28	HV IMON positive input
	ASC_HVMON	18	TP29	Dual Function: HV IMON negative input and VMON10 input

The VCC_CORE current measurement is designed according to Figure 8.3.

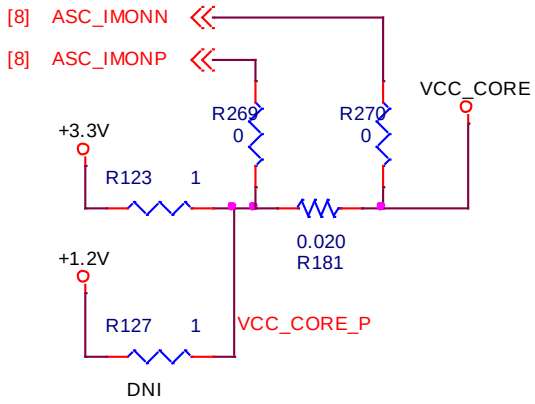

Figure 8.3. VCC Core Current Monitoring Circuit

8.4. ASC Temperature Monitor

The ASC has two external Temperature Monitors (TMONs) that both are connected to on-board temperature sensors, as listed in Table 8.4. One TMON is connected to a PNP transistor, as shown in Figure 8.4. The other TMON is connected to an NPN transistor, as shown in Figure 8.5. Note that the noise suppression capacitors (C33 and C34) shown on the schematic are close to the transistors. However, they are physically close to the L-ASC10 (U7).

Table 8.4. ASC TMON Connections

Temperature Sensor (Reference)	ASC Signal Name	ASC Pin Number	ASC Breakout Test Point	Comments
Temperature Sensor 1 (Q1)	TEMP_SENSE1P	21	TP32	PNP Type
	TEMP_SENSE1N	22	TP33	
Temperature Sensor 2 (Q2)	TEMP_SENSE2P	23	TP34	NPN Type
	TEMP_SENSE2N	24	TP35	

Figure 8.4. PNP Temperature Sensor Circuit

Figure 8.5. NPN Temperature Sensor Circuit

8.5. ASC LEDs

As shown in Figure 8.6, there are nine red LEDs to support ASC applications. They are connected to the ASC GPIOs as listed in Table 8.5. The LEDs illuminate when the GPIO is driven low.

Figure 8.6. ASC LEDs

Table 8.5. GPIO LED Connections

Signal Name	ASC Pin Number	LED	Breakout Test Point	Logic Level to Light
ASC_LED1	44	D9	TP44	0
ASC_LED2	45	D10	TP45	0
ASC_LED3	46	D11	TP46	0
ASC_LED4	47	D12	TP47	0
ASC_LED5	48	D13	TP48	0
ASC_LED6	1	D14	TP49	0
ASC_LED8	11	D15	TP50	0
ASC_LED9	12	D16	TP51	0
ASC_LED10	13	D17	TP52	0

Caution: The MachXO3D Development Board contains ESD-sensitive components. ESD safe practices should be followed while handling and using the development board.

Note: The LEDs are lined up in sequence, as shown in Figure 8.6.

8.6. ASC HVOUT and Trim Pins

The ASC has four high-voltage charge-pump outputs (HVOUTs) and four Trim-DAC outputs (TRIMs), which are brought out to test pins for user convenience, as listed in Table 8.6. The HVOUTs are designed to drive the gates of MOSFETs to enable circuits and loads. The TRIMs are designed to drive the trim inputs of DC-DC converters to adjust the output voltage.

Table 8.6. ASC HVOUT and Trim Connections

Signal Name	ASC Pin Number	Breakout Test Point
ASC_HVOUT1	2	TP40
ASC_HVOUT2	3	TP41
ASC_HVOUT3	9	TP42
ASC_HVOUT4	10	TP43
ASC_TRIM1	39	TP36
ASC_TRIM2	40	TP37
ASC_TRIM3	41	TP38
ASC_TRIM4	42	TP39

9. Software Requirements

The following software are required to develop designs for the MachXO3D Development Board:

- Diamond 3.11 (or later version)
- Diamond Programmer 3.11 (or later version)
- LatticeMico System Development Tools (Optional)

Note: L-ASC device is not supported in Diamond 3.11 SP2 or earlier. Check www.latticesemi.com for the latest news on MachXO3D + ASC support.

10. Storage and Handling

Static electricity can shorten the life span of electronic components. Observe these tips to prevent damage that can occur from electrostatic discharge:

- Use antistatic precautions such as operating on an antistatic mat and wearing an antistatic wristband.
- Store the MachXO3D Development Board in the provided packaging.
- Touch a metal USB housing to equalize voltage potential between you and the board.

11. Ordering Information

Table 11.1 Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
MachXO3D Development Board	LCMXO3D-9400HC-D-EVN	

12. Errata

There is one known issue on the MachXO3D Development Board.

Silk ink for the Raspberry Pi J6 Header (1, 2, 39, 40) should be swapped. Figure 12.1 shows the correct order.

Figure 12.1. Top view of Raspberry Pi Connector

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Appendix A. MachXO3D-9400 Development Board Schematics

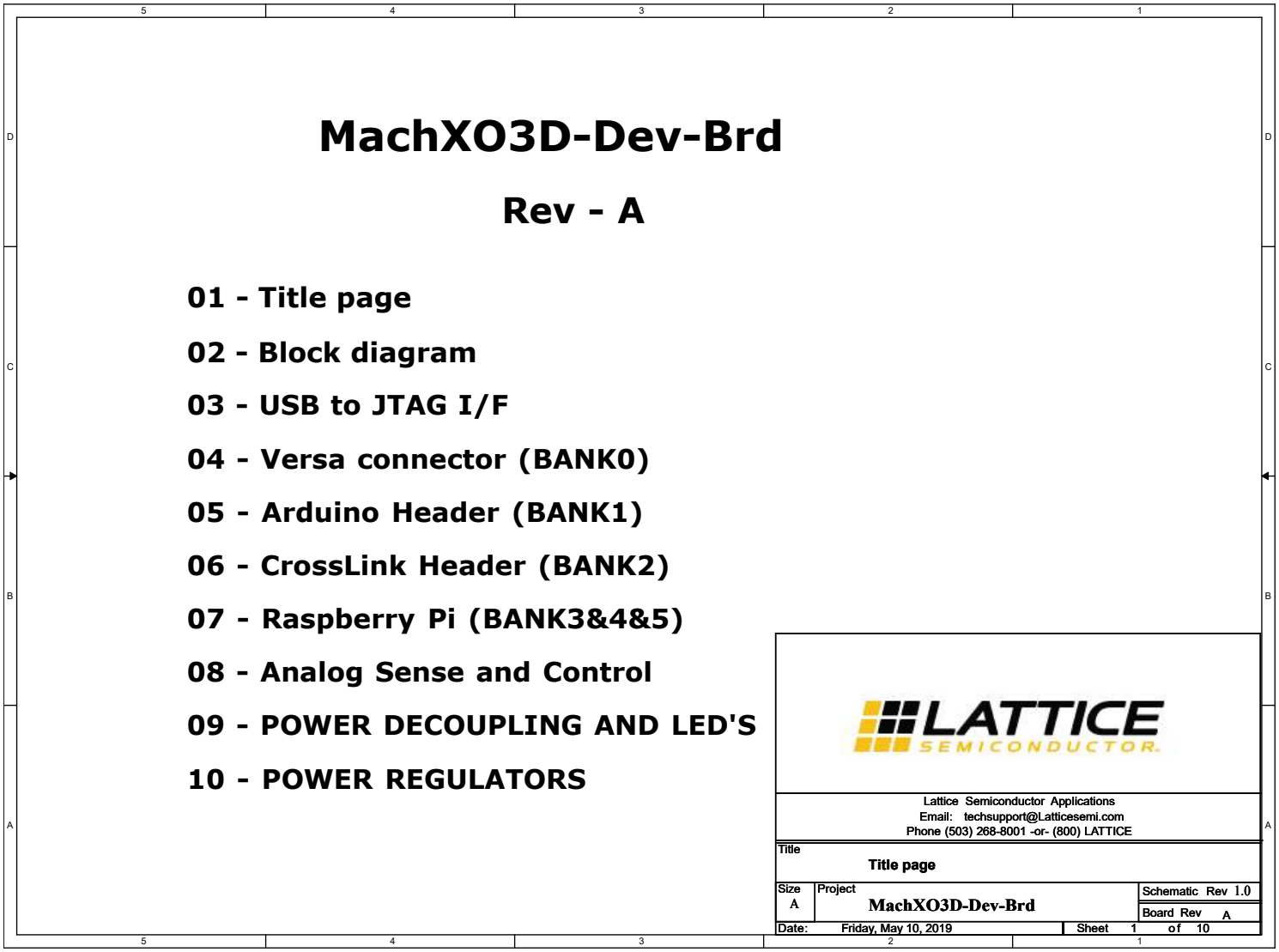

Figure A.1. Title Page

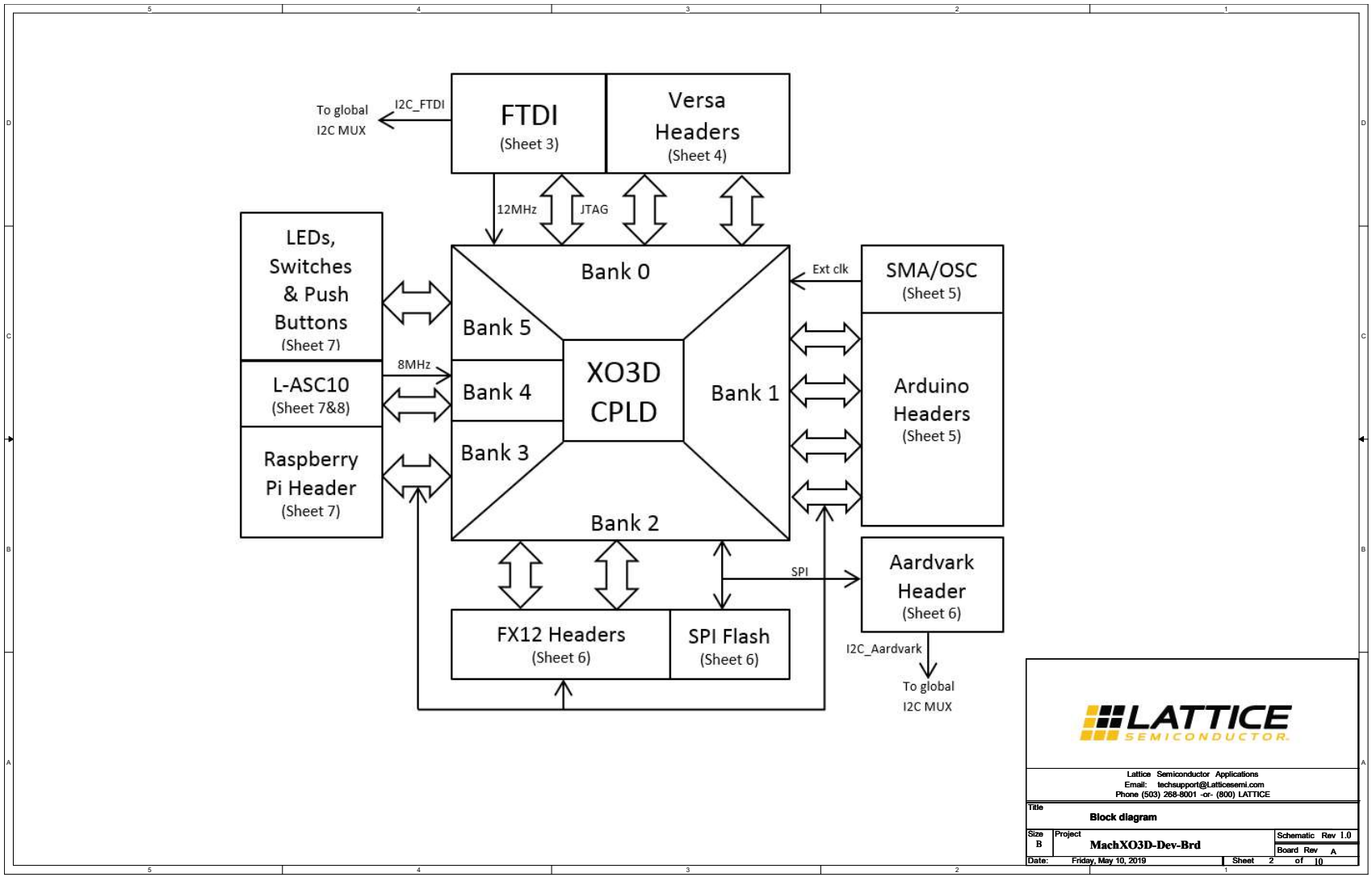

Figure A.2. Block Diagram

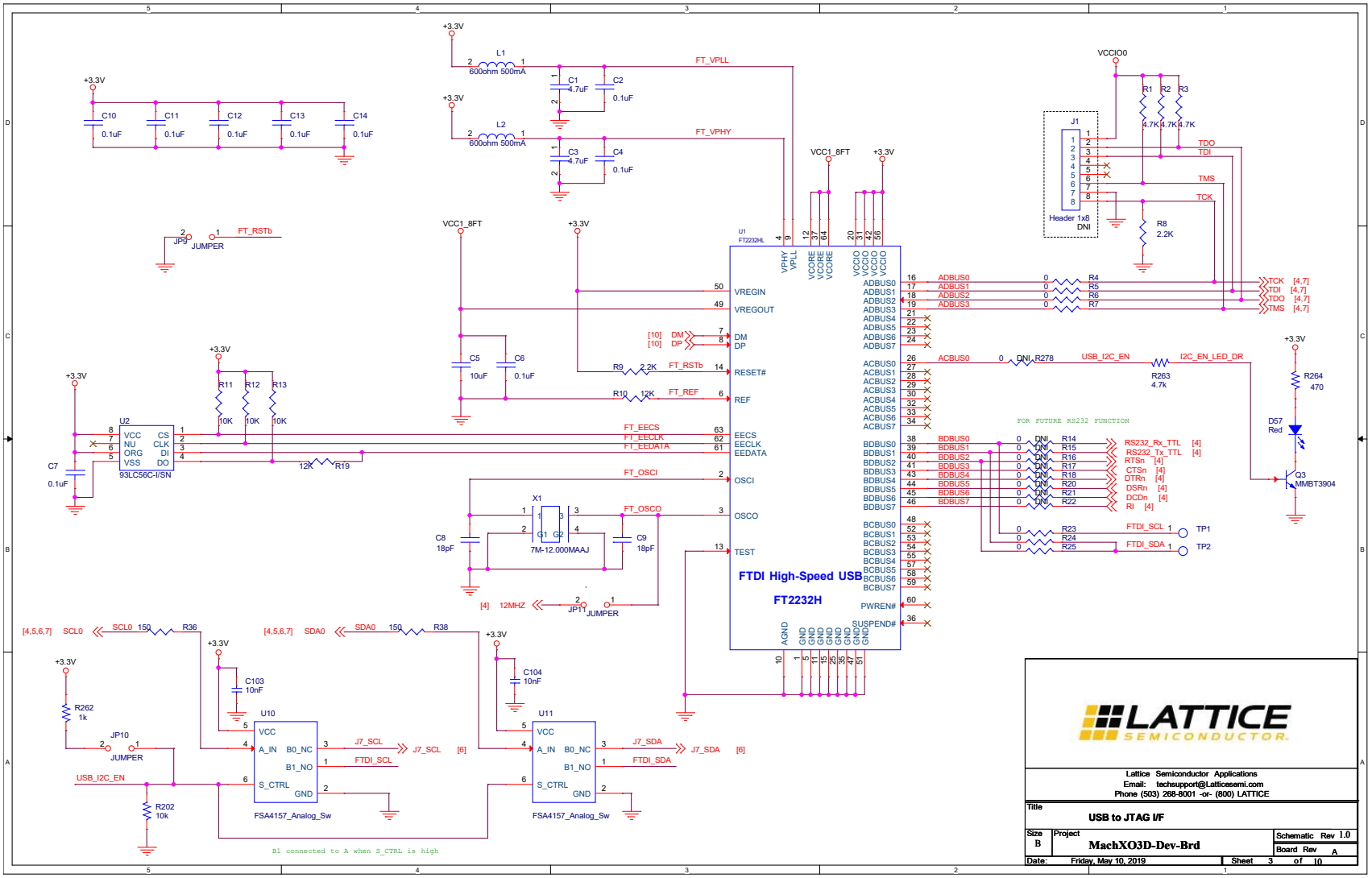

Figure A.3. USB to JTAG I/F

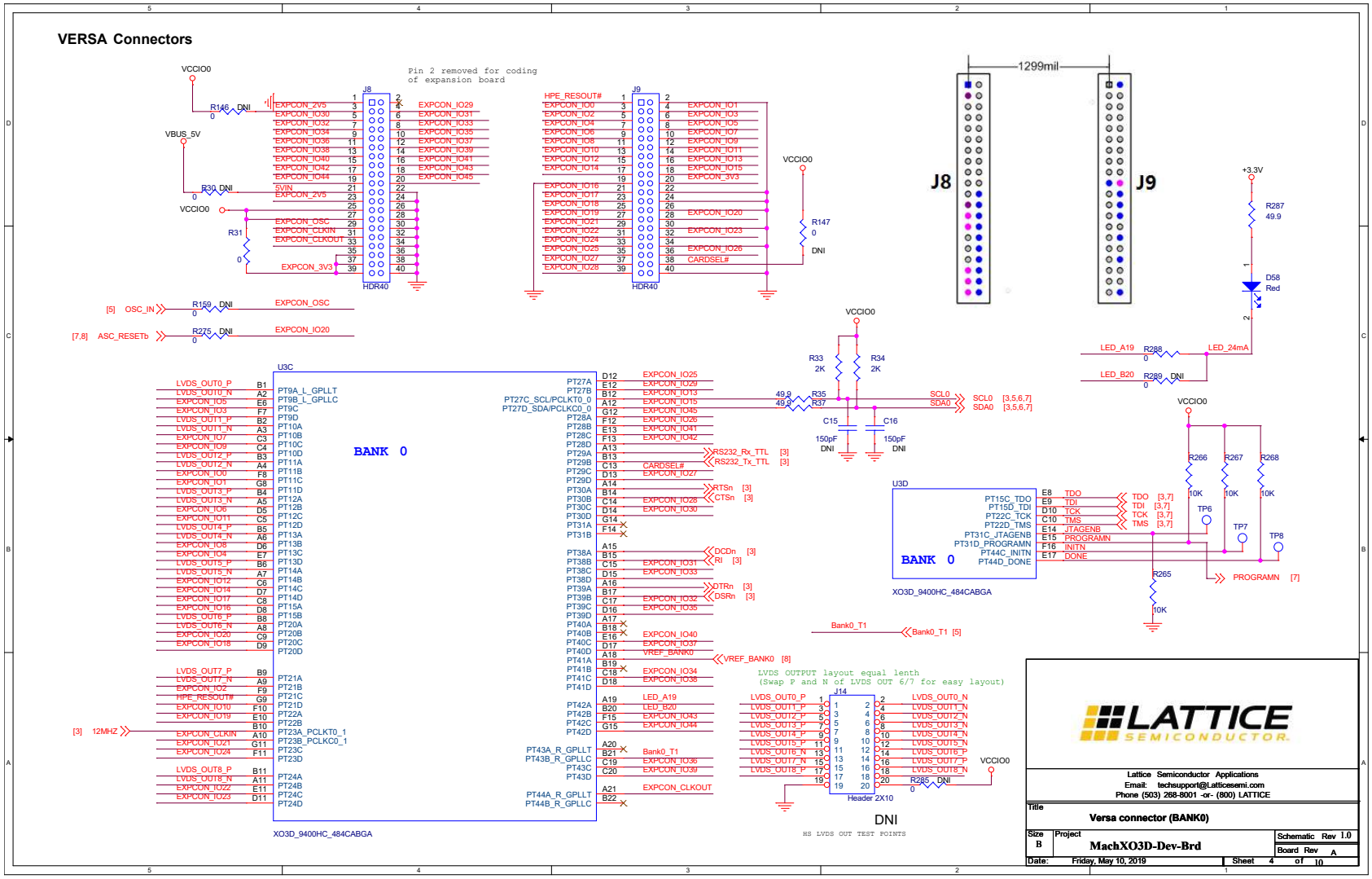

Figure A.4. VERSA Connector (BANK0)

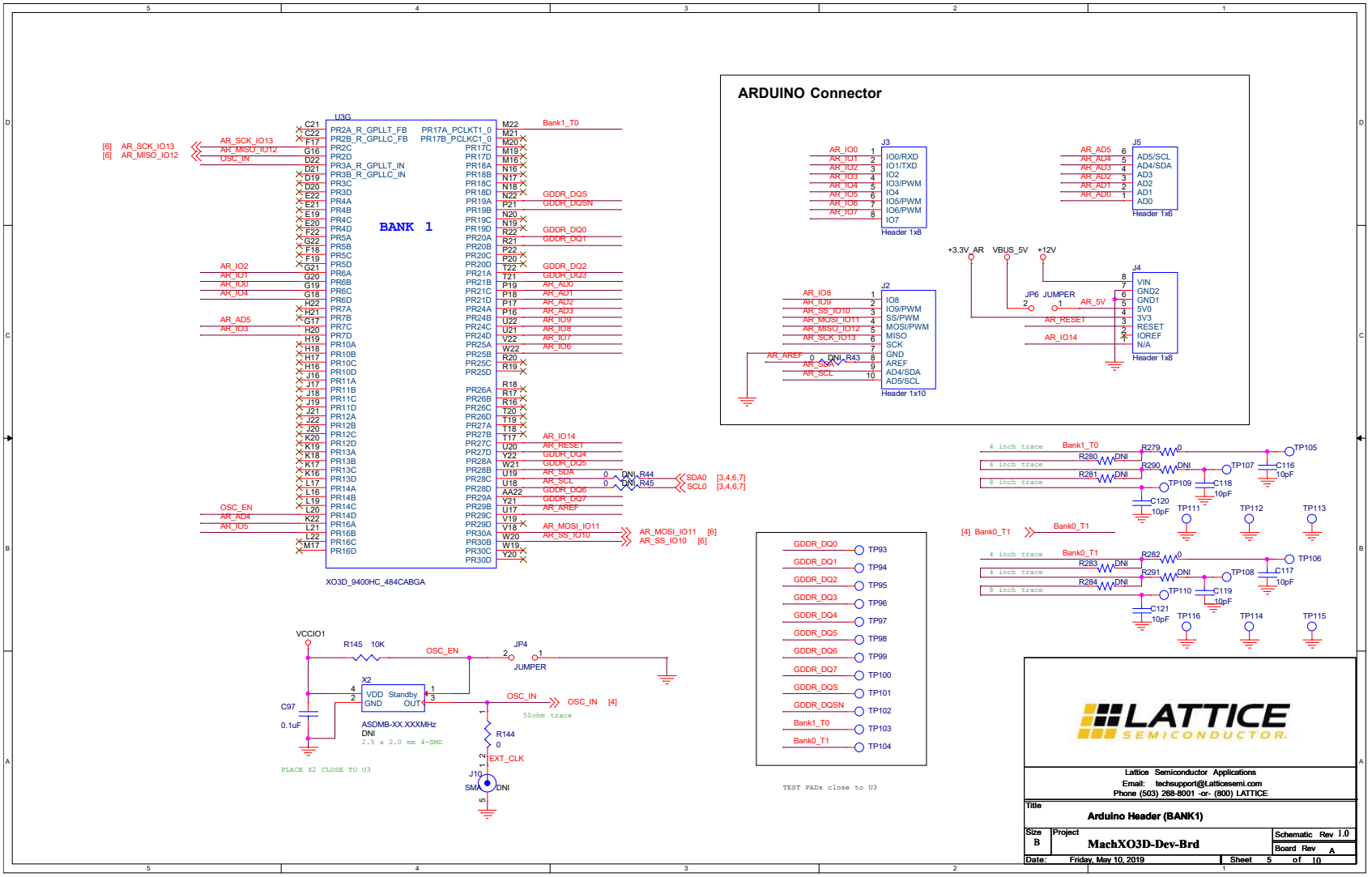

Figure A.5. Arduino Header (BANK1)

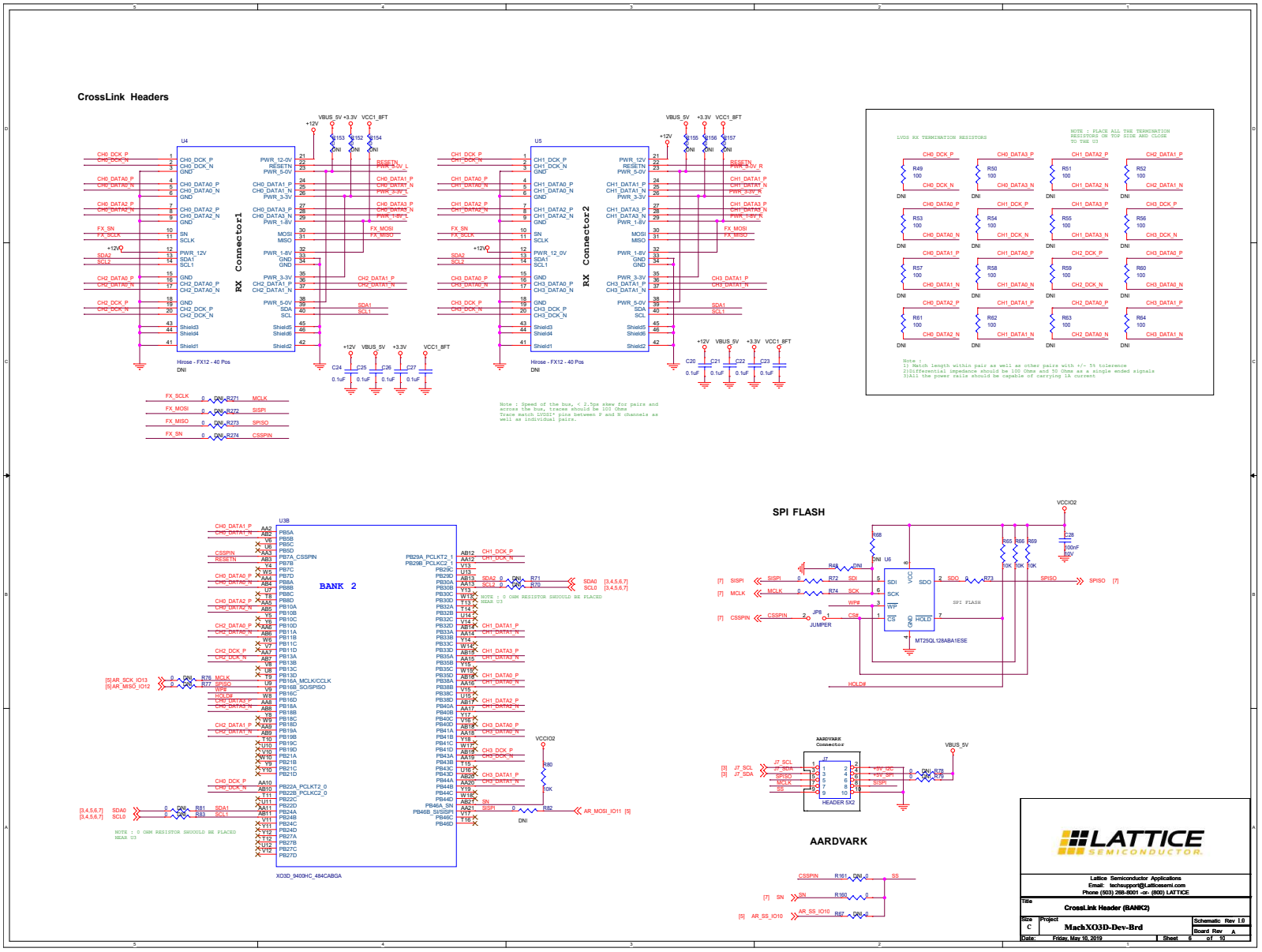

Figure A.6. CrossLink Header (BANK2)

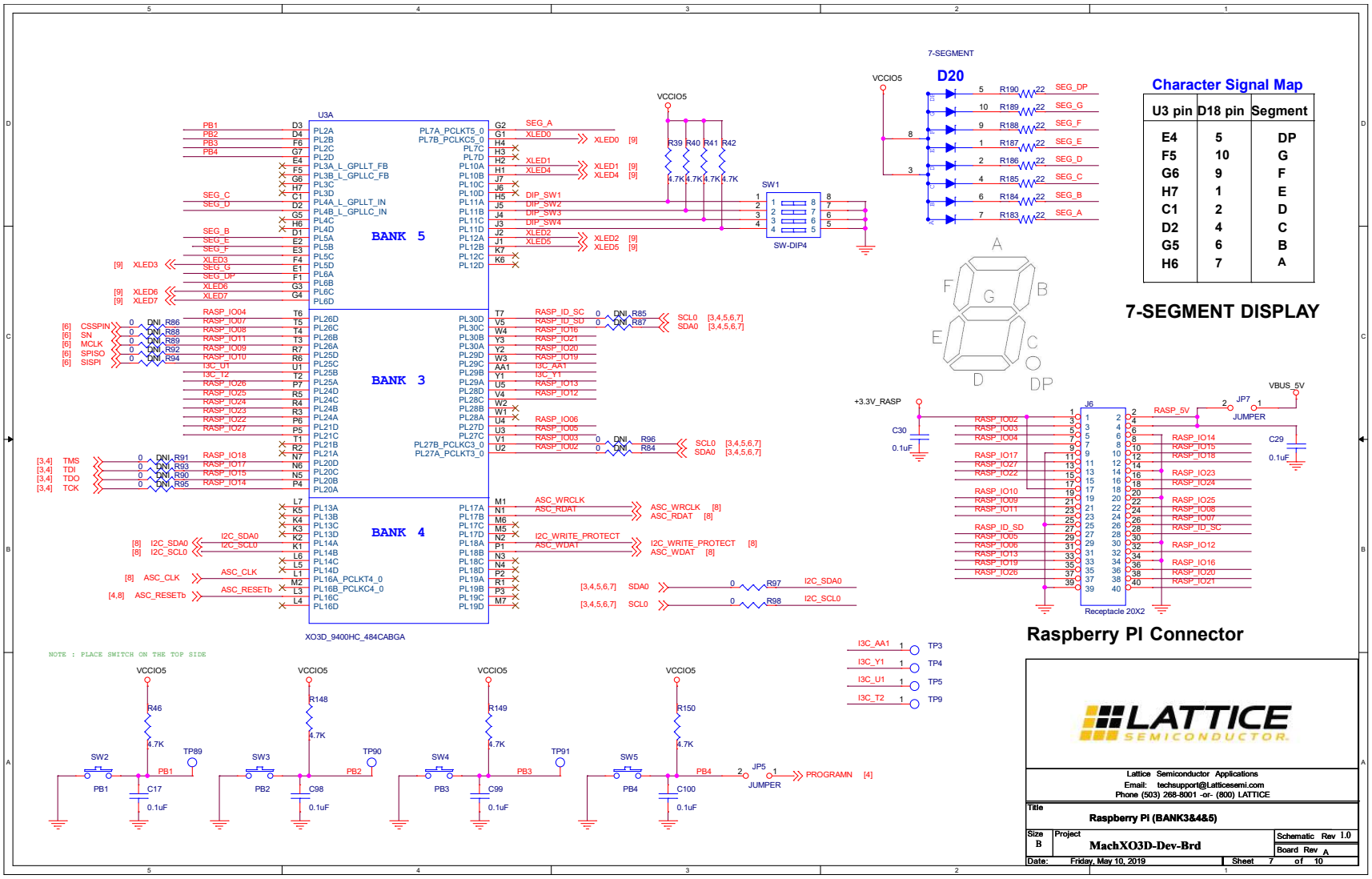

Figure A.7. Raspberry Pi Header and Others (BANK3, BANK4, and BANK5)

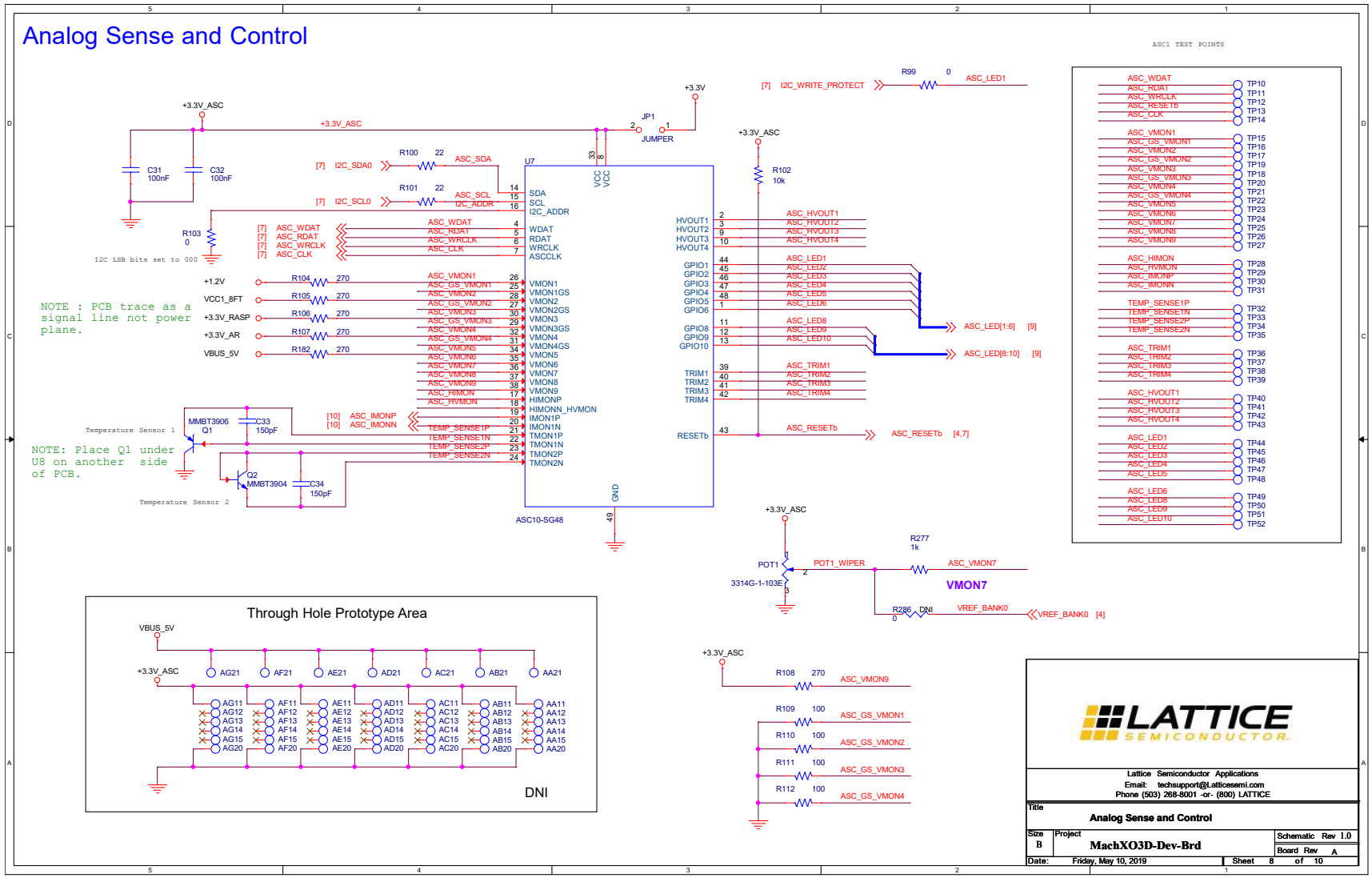

Figure A.8. Analog Sense and Control

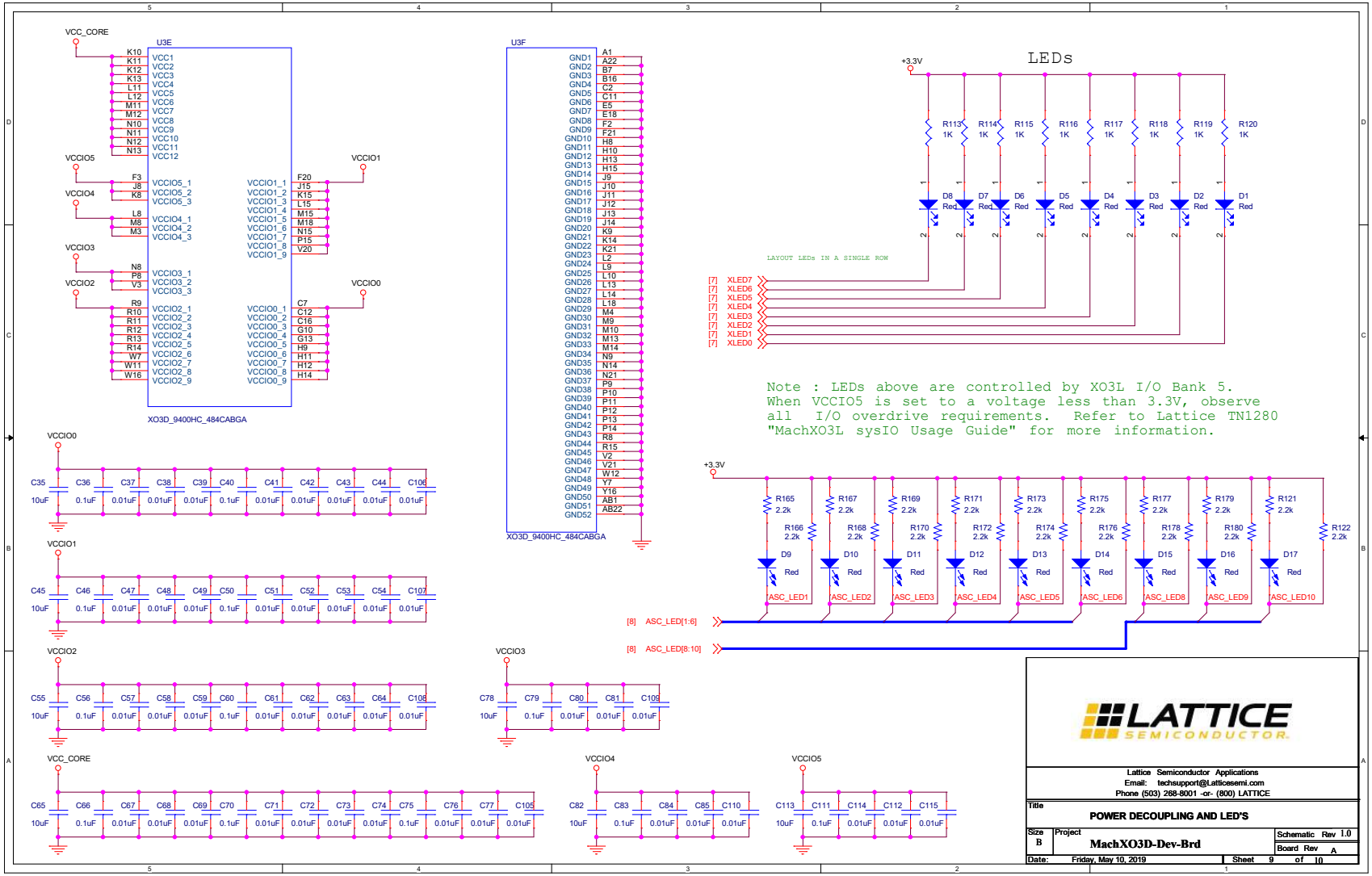

Figure A.9. Power Decoupling and LEDs

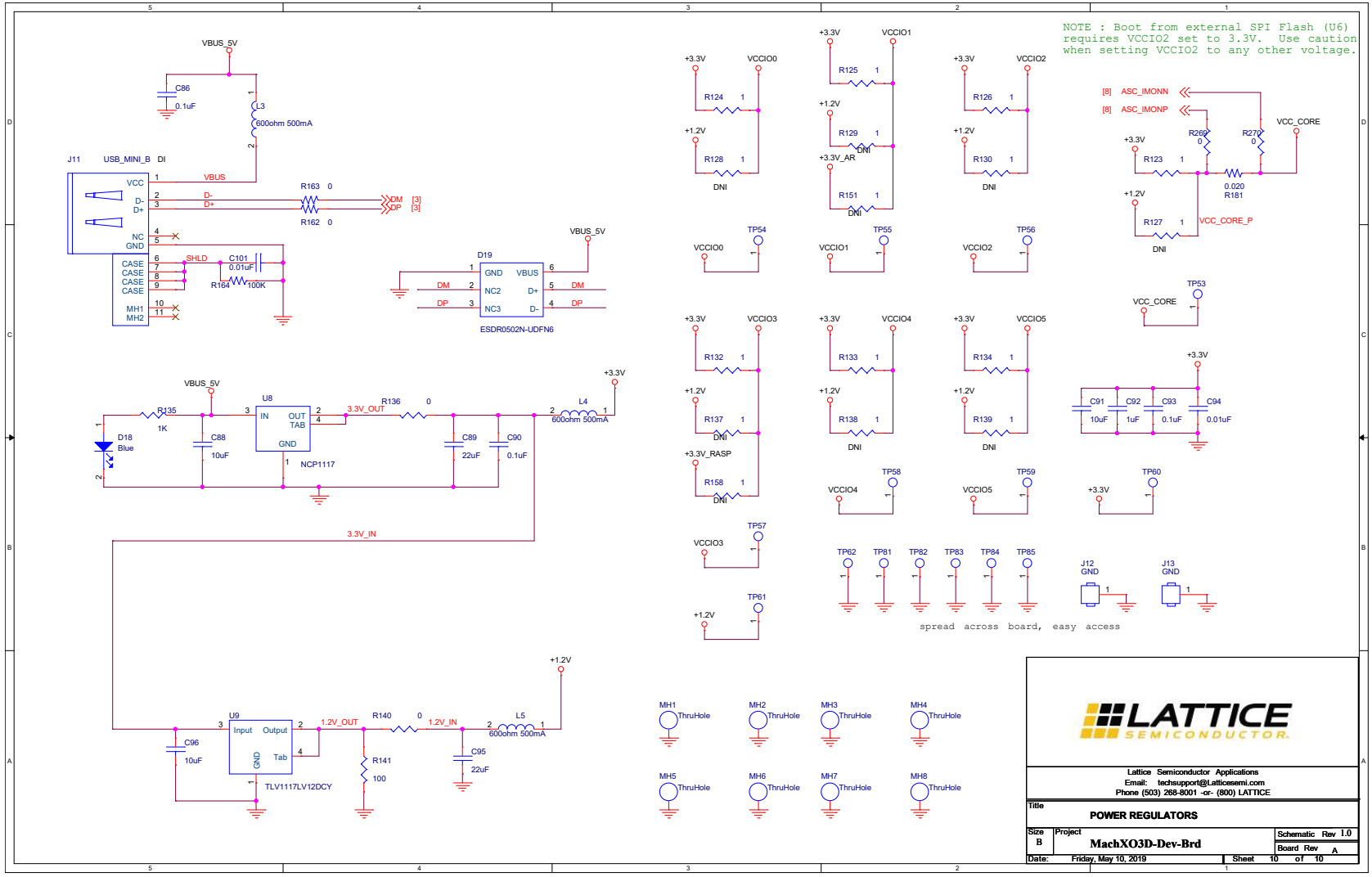

Figure A.10. Power Regulators

Appendix B. MachXO3D-9400 Development Board Bill of Materials

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description	Assembly
1	AG11,AF11,AE11, AD11,AC11,AB11, AA11,AG12,AF12, AE12,AD12,AC12, AB12,AA12,AG13, AF13,AE13,AD13, AC13,AB13,AA13, AG14,AF14,AE14, AD14,AC14,AB14, AA14,AG15,AF15, AE15,AD15,AC15, AB15,AA15,AG20, AF20,AE20,AD20, AC20,AB20,AA20, AG21,AF21,AE21, AD21,AC21,AB21, AA21	49	T POINT R	TP	—	—	—	DNI
2	C1,C3	2	4.7uF	C0603	CL10A475KA8NQNC	Samsung	CAP CER 4.7UF 6.3V 10% X5R 0603	—
3	C2,C4,C6,C7,C10,C 11,C12,C13,C14,C 17,C20,C21,C22,C 23,C24,C25,C26,C 27,C28,C29,C30,C 86,C90,C93,C97,C 98,C99,C100	28	0.1uF	C0402	C1005X5R1E104K05 0BC	TDK	CAP CER 0.1UF 25V 10% X5R 0402	—
4	C5,C35,C45,C55,C 65,C78,C82,C88,C 91,C96,C113	11	10uF	C0603	LMK107BBJ106MAL T	Taiyo Yuden	CAP CER 10UF 10V 20% X5R 0603	—
5	C8,C9	2	18pF	C0402	C0402C180K3GAC7 867	KEMET	CAP CER 18PF 25V 10% NP0 0402	—
6	C15,C16	2	150pF	C0402	—	—	CAP CER 0.1UF 16V 10% X7R 0402	DNI
7	C31,C32	2	100nF	C0603	CL10B104KA8NNNC	Samsung	—	—
8	C33,C34	2	150pF	C0603	CL10B151KB8NNNC	Samsung	—	—
9	C36,C40,C46,C50, C56,C60,C66,C70, C75,C79,C83,C111	12	0.1uF	C0201	C0603X5R1E104K03 0BB	TDK	CAP CER 0.1UF 25V 10% X5R 0201	—

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description	Assembly
10	C37,C38,C39,C41, C42,C43,C44,C47, C48,C49,C51,C52, C53,C54,C57,C58, C59,C61,C62,C63, C64,C67,C68,C69, C71,C72,C73,C74, C76,C77,C80,C81, C84,C85,C105, C106,C107,C108, C109,C110,C112, C114,C115	43	0.01uF	C0201	GRM033R61E103KA 12D	Murata	CAP CER 10000PF 16V 10% X7R 0201	—
11	C89,C95	2	22uF	cc0805	C2012X5R1C226K12 5AC	TDK	CAP CER 22UF 16V 10% X5R 0805	—
12	C92	1	1uF	C0402	CGB2A3X5R0J105K0 33BB	TDK	CAP CER 1UF 6.3V 10% X5R 0402	—
13	C94,C101	2	0.01uF	C0402	CL05B103KA5NNNC	Samsung	CAP CER 10000PF 16V 5% X7R 0402	—
14	C103,C104	2	10nF	C0603	CL10A103KB8NNNC	Samsung	-	—
15	C116,C117,C118,C 119,C120,C121	6	10pF	C0402	-	-	CAP CER 10PF 25V 10% NP0 0402	
16	D1,D2,D3,D4,D5, D6,D7,D8,D9,D10, D11,D12,D13,D14, D15,D16,D17,D57, D58	19	Red	led_0603	LTST-C190KRKT	LITE-On INC	LED RED CLEAR 0603 SMD	—
17	D18	1	Blue	led_0603	LTST-C190TBKT	LITE-On INC	LED 468NM BLUE CLEAR 0603 SMD	—
18	D19	1	ESDR0502 N-UDFN6	UDFN6_040	ESDR0502NMUTBG	ON semi	TVS DIODE 5.5VWM 6UDFN	—
19	D20	1	XZFBBA05 A	LED10-057-394-XZFBBA05A	XZFBBA05A	SunLED	DISPLAY LED 0.2" BLUE CA SMD	—
20	J1	1	Header 1x8	hdr_amp_87 220_8_1x8_ 100	22284081	Molex	CONN HEADER 8POS .100 VERT TIN	DNI
21	J2	1	Header 1x10	CONF1X10-254P_2612X 240X850H_T H	—	—	CONN HEADER 10POS .100 VERT TIN	—

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description	Assembly
22	J3,J4	2	Header 1x8	CONF1X8-254P_2104X240X850H_TH	—	—	CONN HEADER 8POS .100 VERT TIN	—
23	J5	1	Header 1x6	CONF1X6-254P_1596X240X850H_TH	—	—	CONN HEADER 6POS .100 VERT TIN	—
24	J6	1	Receptacle 20X2	HDR254-2X20_socket	PPTC202LFBN-RC	Sullins	CONN HEADER FEM 40POS .1" DL TIN	—
25	J7	1	HEADER 5X2	HDR254-2X5_SHROUDED	30310-6002HB	3M	CONN HEADER 2.54MM 10POS GOLD	DNI
26	J8,J9	2	HDR40	HDR-20x2	—	—	CON M 20x2 THT RM2.54	—
27	J10	1	SMA	bnc5-100-280t	5-1814832-1	TE Connectivity	CONN SMA JACK STR 50 OHM PCB	DNI
28	J11	1	USB_MINI_B	usb2-0-rec-240-0001-9	UX60-MB-5ST	Hirose	CONN RECEPT MINI USB2.0 5POS	—
29	J12, J13	2	GND	TUR_TH	1573-2	Keystone Electronics	TERMINAL TURRET DBL .082"L	—
30	J14	1	HEADER 10X2	HDR254-2X10	—	—	CONN HEADER 20POS .100" STR	DNI
31	JP1,JP4,JP5,JP6, JP7,JP8,JP9,JP10, JP11	9	JUMPER	Header_1x2	—	—	CONN HEADER 2POS .100 VERT TIN	—
32	L1,L2,L3,L4,L5	5	600ohm 500mA	fb0603	BLM18AG601SN1D	Murata	FERRITE CHIP 600 OHM 500MA 0603	—
33	POT1	1	3314G-1-103E	sot23-3314G-1	3314G-1-103E	Bourns Inc.	TRIMMER 10K OHM 0.25W SMD	—
34	Q1	1	MMBT3906	MMBT3906	MMBT3906	ON Semiconductor	TRANS PNP 40V 0.2A SOT-23	—
35	Q2,Q3	2	MMBT3904	MMBT3904	MMBT3904	ON Semiconductor	TRANS NPN 40V 0.2A SOT-23	—

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description	Assembly
36	R1,R2,R3,R39,R40, R41,R42,R46, R148,R149, R150,R263	12	4.7k	R0603	RC0603FR-074K7L	Yageo	RES 4.70K OHM 1/10W 1% 0603 SMD	—
37	R4,R5,R6,R7,R23,R 24,R25,R31,R72,R 73,R74,R97,R98,R 99,R103,R136,R14 0,R160,R269,R270 ,R279,R282,R288	23	0	R0603	RC0603FR-070RL	Yageo	RES 0.0 OHM 1/10W JUMP 0603 SMD	—
38	R8,R9,R121,R122, R165,R166,R167, R168,R169,R170, R171,R172,R173, R174,R175,R176, R177,R178,R179, R180	20	2.2k	R0603	RC0603FR-072K2L	Yageo	—	—
39	R10,R19	2	12K	R0603	RC0603FR-0712KL	Yageo	RES 12K OHM 1/10W 1% 0603 SMD	—
40	R11,R12,R13, R65,R66,R69,R80, R102,R145,R202,R 265,R266,R267,R2 68	14	10K	R0603	RC0603FR-0710KL	Yageo	RES 10K OHM 1/10W 5% 0603	—
41	R14,R15,R16,R17, R18,R20,R21,R22, R30,R43,R44,R45, R67,R70,R71,R76, R77,R78,R79,R81, R82,R83,R84,R85, R86,R87,R88,R89, R90,R91,R92,R93, R94,R95,R96,R146 ,R147,R152,R153, R154,R155,R156,R 157,R159,R161,R2 71,R272,R273,R27 4,R275,R278,R280 ,R281,R283,R284, R285,R286,R289,R 290,R291	60	0	R0603	—	—	RES 0.0 OHM 1/10W JUMP 0603 SMD	DNI
42	R33,R34	2	2K	R0603	RC0603FR-072KL	Yageo	RES 2.0K OHM 1/10W 5% 0603 SMD	—
43	R35,R37,R287	3	49.9	R0603	RC0603FR-0749R9L	Yageo	RES 49.9 OHM 1/10W 1% 0603 SMD	—
44	R36,R38	2	150	R0603	RC0603FR-07151RL	Yageo	RES 150 OHM 1/10W 5% 0603 SMD	—

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description	Assembly
45	R49,R50,R51,R52, R53,R54,R55,R56, R57,R58,R59,R60, R61,R62,R63,R64	16	100	R0402	—	—	RES SMD 100 OHM 1% 1/16W 0402	DNI
46	R48, R68	1	1K	R0603	—	—	—	DNI
47	R100,R101,R183,R184,R185,R186,R187,R188,R189,R190	10	22	R0603	RC0603FR-0722RL	Yageo	—	—
48	R104,R105,R106, R107,R108,R182	6	270	R0603	RC0603FR-07270RL	Yageo	—	—
49	R109,R110,R111, R112,R141	5	100	R0603	RC0603FR-07100RL	Yageo	—	—
50	R113,R114, R115,R116,R117, R118,R119,R120, R135,R262,R277	11	1k	R0603	RC0603FR-071KL	Yageo	RES 1K OHM 1/10W 1% 0603 SMD	—
51	R123,R124,R125, R126,R132,R133, R134	7	1	R0603	RC0603FR-071RL	Yageo	RES 1.0 OHM .25W 5% 0603 SMD	—
52	R127,R128,R129, R130,R137,R138, R139,R151,R158	9	1	R0603	RC0603FR-071RL	Yageo	RES 1.0 OHM .25W 5% 0603 SMD	DNI
53	R144,R162,R163	3	0	R0402	RC0402FR-070RL	Yageo	—	—
54	R164	1	100K	R0603	RC0603FR-07100KL	Yageo	—	—
55	R181	1	0.02	SM_R_ 1206	RL1206FR-070R02L	Yageo	—	—
56	R264	1	470	R0603	RC0603FR-07470RL	Yageo	—	—
57	SW1	1	SW-DIP4	sw_sp_st_ cts_195-4mst	195-4MST	CTS	SWITCH PIANO DIP SPST 50MA 24V	—
58	SW2,SW3,SW4,SW5	4	Push Button	sw_sp_st_ eswitch_ tl1015	TL1015AF160QG	E-Switch	SWITCH TACTILE SPST-NO 0.05A 12V	—

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description	Assembly
59	TP1,TP2,TP3,TP4,TP5,TP6,TP7,TP8,TP9,TP10,TP11,TP12,TP13,TP14,TP15,TP16,TP17,TP18,TP19,TP20,TP21,TP22,TP23,TP24,TP25,TP26,TP27,TP28,TP29,TP30,TP31,TP32,TP33,TP34,TP35,TP36,TP37,TP38,TP39,TP40,TP41,TP42,TP43,TP44,TP45,TP46,TP47,TP48,TP49,TP50,TP51,TP52,TP53,TP54,TP55,TP56,TP57,TP58,TP59,TP60,TP61,TP62,TP81,TP82,TP83,TP84,TP85,TP89,TP90,TP91	70	T POINT R	TP	-	-	Square test point, 40mil inner diameter, 63mil outer diameter	DNI
60	TP93,TP94,TP95,TP96,TP97,TP98,TP99,TP100,TP101,TP102,TP103,TP104,TP105,TP106,TP107,TP108,TP109,TP110,TP111,TP112,TP113,TP114,TP115,TP116	24	T POINT R	TPC32				
61	U1	1	FT2232HL	tqfp64_0p5_12p2x12p2_h1p6	FT2232HL-TRAY	FTDI	IC USB HS DUAL UART/FIFO 64-LQFP	—
62	U2	1	93LC56C-I/SN	so8_50_244	93LC56C-I/SN	Microchip	IC EEPROM 2KBIT 3MHZ 8SOIC	—
63	U3	1	XO3D_9400HC_484CABGA	BGA484-080	XO3D_9400HC_484CABGA	Lattice	XO3D-HC9400 device	—
64	U4,U5	2	Hirose - FX12 - 40 Pos	Hirose-FX12	FX12B-40P-0.4SV	Hirose	CONN PLUG 40POS 0.4MM SMD SHIELD	DNI
65	U6	1	MT25QL128ABA1ESE	sop8-50-208	MT25QL128ABA1ESE-0SIT	Micron	IC FLASH 128MBIT 133MHZ 8SOW	—
66	U7	1	ASC10-SG48	TQFN_48	L-ASC10-1SG48I	Lattice	ASC Device	—
67	U8	1	NCP1117	sot223_4p	NCP1117ST33T3G	ON semi	IC REG LDO 3.3V 1A SOT223	—

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description	Assembly
68	U9	1	TLV1117LV12DCY	sot223_4p	TLV1117LV12DCY	TI	IC REG LDO 1.2V 1A SOT223-3	—
69	U10,U11	2	FSA4157_Analog_Sw	SOP-6-26	FSA4157P6X	Fairchild	IC SWITCH SPDT SC70-6	—
70	X1	1	7M-12.000MAAJ	xtal_4p_7m	7M-12.000MAAJ-T	TXC	CRYSTAL 12MHZ 18PF SMD	—
71	X2	1	ASDMB-XX.XXXMHz	x4-2520	ASDMB serial	Abracon LLC	OSC MEMS CMOS SMD	DNI

Appendix C. Predefined Preference File Listing

```
// These names are generated by the Platform Designer tool in Diamond software
// and can be copied into the preference file or entered into the Spreadsheet
// view.

// ASC0 Connections
LOCATE COMP "ASC0_RSTN" SITE "L3" ;
LOCATE COMP "ASC0_CLK"  SITE "L1" ;
LOCATE COMP "rdat_0"    SITE "N1" ;
LOCATE COMP "wdat_0"    SITE "P1" ;
LOCATE COMP "wrclk_0"   SITE "M1" ;
```

Appendix D. User Defined Preference File Listing

```
// These names follow the MachXO3D Development Board schematic but,
// they may be defined by the user.  Thus, they can be copied into the
// preference file and edited to match a different naming convention if
// needed or used to fill in the Spreadsheet view.

// XO3D LED Connections
// Note: The following order matches the LED locations on the board
// from top to bottom
LOCATE COMP "XLED3" SITE "F4" ;
LOCATE COMP "XLED7" SITE "G4" ;
LOCATE COMP "XLED6" SITE "G3" ;
LOCATE COMP "XLED0" SITE "G1" ;
LOCATE COMP "XLED1" SITE "H2" ;
LOCATE COMP "XLED4" SITE "H1" ;
LOCATE COMP "XLED2" SITE "J2" ;
LOCATE COMP "XLED5" SITE "J1" ;

// XO3D High Current LED
LOCATE COMP "LED_A19"  SITE "A19" ;
LOCATE COMP "LED_B20"  SITE "B20" ;

// XO3D DIP Switch Connections
LOCATE COMP "DIP_SW1" SITE "H5" ;
LOCATE COMP "DIP_SW2" SITE "J5" ;
LOCATE COMP "DIP_SW3" SITE "J4" ;
LOCATE COMP "DIP_SW4" SITE "J3" ;

// XO3D SEG LED Connections
LOCATE COMP "SEG_DP" SITE "F1" ;
LOCATE COMP "SEG_G" SITE "E1" ;
LOCATE COMP "SEG_F" SITE "E3" ;
LOCATE COMP "SEG_E" SITE "E2" ;
LOCATE COMP "SEG_D" SITE "D2" ;
LOCATE COMP "SEG_C" SITE "C1" ;
LOCATE COMP "SEG_B" SITE "D1" ;
LOCATE COMP "SEG_A" SITE "G2" ;

// XO3D Push Button Switch Connections
LOCATE COMP "PB1" SITE "D3" ;
LOCATE COMP "PB2" SITE "D4" ;
LOCATE COMP "PB3" SITE "F6" ;
LOCATE COMP "PB4" SITE "G7" ;

// XO3D I3C Connections
LOCATE COMP "I3C_SDA0"   SITE "AA1" ;
LOCATE COMP "I3C_SCL0"   SITE "Y1" ;
LOCATE COMP "I3C_SDA1"   SITE "U1" ;
LOCATE COMP "I3C_SCL1"   SITE "T2" ;

// XO3D SPI Flash Connections
LOCATE COMP "CSSPIN" SITE "AA3" ;
LOCATE COMP "MCLK"   SITE "T9" ;
LOCATE COMP "SISPI"  SITE "AA21" ;
LOCATE COMP "SPISO"  SITE "U9" ;
LOCATE COMP "WP#"    SITE "V9" ;
LOCATE COMP "HOLD#"  SITE "W8" ;
```

```
// XO3D Slew Rate Test Points
LOCATE COMP "Bank0_T1"  SITE "B21" ;
LOCATE COMP "Bank1_T0"  SITE "M22" ;

// XO3D ARDUINO Connections
LOCATE COMP "AR_AD0"  SITE "P19" ;
LOCATE COMP "AR_AD1"  SITE "P18" ;
LOCATE COMP "AR_AD2"  SITE "P17" ;
LOCATE COMP "AR_AD3"  SITE "P16" ;
LOCATE COMP "AR_AD4"  SITE "K22" ;
LOCATE COMP "AR_AD5"  SITE "G17" ;
LOCATE COMP "AR_IO0"  SITE "G19" ;
LOCATE COMP "AR_IO1"  SITE "G20" ;
LOCATE COMP "AR_IO2"  SITE "G21" ;
LOCATE COMP "AR_IO3"  SITE "H20" ;
LOCATE COMP "AR_IO4"  SITE "G18" ;
LOCATE COMP "AR_IO5"  SITE "L21" ;
LOCATE COMP "AR_IO6"  SITE "W22" ;
LOCATE COMP "AR_IO7"  SITE "V22" ;
LOCATE COMP "AR_IO8"  SITE "U21" ;
LOCATE COMP "AR_IO9"  SITE "U22" ;
LOCATE COMP "AR_SS_IO10"   SITE "W20" ;
LOCATE COMP "AR_MOSI_IO11" SITE "V18" ;
LOCATE COMP "AR_MISO_IO12" SITE "G16" ;
LOCATE COMP "AR_SCK_IO13"  SITE "F17" ;
LOCATE COMP "AR_IO14"      SITE "T17" ;
LOCATE COMP "AR_AREF"      SITE "U17" ;
LOCATE COMP "AR_SDA"       SITE "U19" ;
LOCATE COMP "AR_SCL"       SITE "U18" ;
LOCATE COMP "AR_RESET"     SITE "U20" ;

// XO3D Raspberry Pi Connections
LOCATE COMP "RASP_IO02"   SITE "U2" ;
LOCATE COMP "RASP_IO03"   SITE "V1" ;
LOCATE COMP "RASP_IO04"   SITE "T6" ;
LOCATE COMP "RASP_IO05"   SITE "U3" ;
LOCATE COMP "RASP_IO06"   SITE "U4" ;
LOCATE COMP "RASP_IO07"   SITE "T5" ;
LOCATE COMP "RASP_IO08"   SITE "T4" ;
LOCATE COMP "RASP_IO09"   SITE "R7" ;
LOCATE COMP "RASP_IO10"   SITE "R6" ;
LOCATE COMP "RASP_IO11"   SITE "T3" ;
LOCATE COMP "RASP_IO12"   SITE "V4" ;
LOCATE COMP "RASP_IO13"   SITE "U5" ;
LOCATE COMP "RASP_IO14"   SITE "P4" ;
LOCATE COMP "RASP_IO15"   SITE "N5" ;
LOCATE COMP "RASP_IO16"   SITE "W4" ;
LOCATE COMP "RASP_IO17"   SITE "N6" ;
LOCATE COMP "RASP_IO18"   SITE "N7" ;
LOCATE COMP "RASP_IO19"   SITE "W3" ;
LOCATE COMP "RASP_IO20"   SITE "Y2" ;
LOCATE COMP "RASP_IO21"   SITE "Y3" ;
LOCATE COMP "RASP_IO22"   SITE "P6" ;
LOCATE COMP "RASP_IO23"   SITE "R3" ;
LOCATE COMP "RASP_IO24"   SITE "R4" ;
LOCATE COMP "RASP_IO25"   SITE "R5" ;
LOCATE COMP "RASP_ID_SD"  SITE "V5" ;
LOCATE COMP "RASP_ID_SC"  SITE "T7" ;
```

```
// XO3D Clock Connections
LOCATE COMP "12MHZ"  SITE "B10" ;
LOCATE COMP "OSC_IN" SITE "D22" ;
LOCATE COMP "OSC_EN" SITE "L20" ;

// XO3D VERSA Connections
LOCATE COMP "EXPCON_IO0"    SITE "F8" ;
LOCATE COMP "EXPCON_IO1"    SITE "G8" ;
LOCATE COMP "EXPCON_IO2"    SITE "F9" ;
LOCATE COMP "EXPCON_IO3"    SITE "F7" ;
LOCATE COMP "EXPCON_IO4"    SITE "E7" ;
LOCATE COMP "EXPCON_IO5"    SITE "E6" ;
LOCATE COMP "EXPCON_IO6"    SITE "D5" ;
LOCATE COMP "EXPCON_IO7"    SITE "C3" ;
LOCATE COMP "EXPCON_IO8"    SITE "D6" ;
LOCATE COMP "EXPCON_IO9"    SITE "C4" ;
LOCATE COMP "EXPCON_IO10"   SITE "F10" ;
LOCATE COMP "EXPCON_IO11"   SITE "C5" ;
LOCATE COMP "EXPCON_IO12"   SITE "C6" ;
LOCATE COMP "EXPCON_IO13"   SITE "B2" ;
LOCATE COMP "EXPCON_IO14"   SITE "D7" ;
LOCATE COMP "EXPCON_IO15"   SITE "A12" ;
LOCATE COMP "EXPCON_IO16"   SITE "D8" ;
LOCATE COMP "EXPCON_IO17"   SITE "C8" ;
LOCATE COMP "EXPCON_IO18"   SITE "D9" ;
LOCATE COMP "EXPCON_IO19"   SITE "E10" ;
LOCATE COMP "EXPCON_IO20"   SITE "C9" ;
LOCATE COMP "EXPCON_IO21"   SITE "G11" ;
LOCATE COMP "EXPCON_IO22"   SITE "E11" ;
LOCATE COMP "EXPCON_IO23"   SITE "D11" ;
LOCATE COMP "EXPCON_IO24"   SITE "F11" ;
LOCATE COMP "EXPCON_IO25"   SITE "D12" ;
LOCATE COMP "EXPCON_IO26"   SITE "F12" ;
LOCATE COMP "EXPCON_IO27"   SITE "D13" ;
LOCATE COMP "EXPCON_IO28"   SITE "C14" ;
LOCATE COMP "EXPCON_IO29"   SITE "E12" ;
LOCATE COMP "EXPCON_IO30"   SITE "D14" ;
LOCATE COMP "EXPCON_IO31"   SITE "C15" ;
LOCATE COMP "EXPCON_IO32"   SITE "C17" ;
LOCATE COMP "EXPCON_IO33"   SITE "D15" ;
LOCATE COMP "EXPCON_IO34"   SITE "C18" ;
LOCATE COMP "EXPCON_IO35"   SITE "D16" ;
LOCATE COMP "EXPCON_IO36"   SITE "C19" ;
LOCATE COMP "EXPCON_IO37"   SITE "D17" ;
LOCATE COMP "EXPCON_IO38"   SITE "D18" ;
LOCATE COMP "EXPCON_IO39"   SITE "C20" ;
LOCATE COMP "EXPCON_IO40"   SITE "E16" ;
LOCATE COMP "EXPCON_IO41"   SITE "E13" ;
LOCATE COMP "EXPCON_IO42"   SITE "F13" ;
LOCATE COMP "EXPCON_IO43"   SITE "F15" ;
LOCATE COMP "EXPCON_IO44"   SITE "G15" ;
LOCATE COMP "EXPCON_IO45"   SITE "G12" ;
LOCATE COMP "EXPCON_OSC"    SITE "D22" ;
LOCATE COMP "EXPCON_CLKIN"  SITE "A10" ;
LOCATE COMP "EXPCON_CLKOUT" SITE "A21" ;
LOCATE COMP "CARDSEL#"      SITE "C13" ;
LOCATE COMP "HPE_RESOUT#"   SITE "G9" ;
```

```
// XO3D LVDS Test Connections
LOCATE COMP "LVDS_OUT0_P"  SITE "B1" ;
LOCATE COMP "LVDS_OUT0_N"  SITE "A2" ;
LOCATE COMP "LVDS_OUT1_P"  SITE "B2" ;
LOCATE COMP "LVDS_OUT1_N"  SITE "A3" ;
LOCATE COMP "LVDS_OUT2_P"  SITE "B3" ;
LOCATE COMP "LVDS_OUT2_N"  SITE "A4" ;
LOCATE COMP "LVDS_OUT3_P"  SITE "B4" ;
LOCATE COMP "LVDS_OUT3_N"  SITE "A5" ;
LOCATE COMP "LVDS_OUT4_P"  SITE "B5" ;
LOCATE COMP "LVDS_OUT4_N"  SITE "A6" ;
LOCATE COMP "LVDS_OUT5_P"  SITE "B6" ;
LOCATE COMP "LVDS_OUT5_N"  SITE "A7" ;
LOCATE COMP "LVDS_OUT6_P"  SITE "B8" ;
LOCATE COMP "LVDS_OUT6_N"  SITE "A8" ;
LOCATE COMP "LVDS_OUT7_P"  SITE "B9" ;
LOCATE COMP "LVDS_OUT7_N"  SITE "A9" ;
LOCATE COMP "LVDS_OUT8_P"  SITE "B11" ;
LOCATE COMP "LVDS_OUT8_N"  SITE "A11" ;

// XO3D GDDR Test Connections
LOCATE COMP "GDDR_DQ0"   SITE "R22" ;
LOCATE COMP "GDDR_DQ1"   SITE "R21" ;
LOCATE COMP "GDDR_DQ2"   SITE "T22" ;
LOCATE COMP "GDDR_DQ3"   SITE "T21" ;
LOCATE COMP "GDDR_DQ4"   SITE "Y22" ;
LOCATE COMP "GDDR_DQ5"   SITE "W21" ;
LOCATE COMP "GDDR_DQ6"   SITE "AA22" ;
LOCATE COMP "GDDR_DQ7"   SITE "Y21" ;
LOCATE COMP "GDDR_DQS"   SITE "N22" ;
LOCATE COMP "GDDR_DQSN"  SITE "P21" ;


// XO3D CrossLink Connections
LOCATE COMP "CH0_DCK_P"    SITE "AA10" ;
LOCATE COMP "CH0_DCK_N"    SITE "AB10" ;
LOCATE COMP "CH0_DATA0_P"  SITE "AA4" ;
LOCATE COMP "CH0_DATA0_N"  SITE "AB4" ;
LOCATE COMP "CH0_DATA1_P"  SITE "AA2" ;
LOCATE COMP "CH0_DATA1_N"  SITE "AB2" ;
LOCATE COMP "CH0_DATA2_P"  SITE "AA5" ;
LOCATE COMP "CH0_DATA2_N"  SITE "AB5" ;
LOCATE COMP "CH0_DATA3_P"  SITE "AA8" ;
LOCATE COMP "CH0_DATA3_N"  SITE "AB8" ;
LOCATE COMP "CH1_DCK_P"    SITE "AB12" ;
LOCATE COMP "CH1_DCK_N"    SITE "AA12" ;
LOCATE COMP "CH1_DATA0_P"  SITE "AB16" ;
LOCATE COMP "CH1_DATA0_N"  SITE "AA16" ;
LOCATE COMP "CH1_DATA1_P"  SITE "AB14" ;
LOCATE COMP "CH1_DATA1_N"  SITE "AA14" ;
LOCATE COMP "CH1_DATA2_P"  SITE "AB17" ;
LOCATE COMP "CH1_DATA2_N"  SITE "AA17" ;
LOCATE COMP "CH1_DATA3_P"  SITE "AB15" ;
LOCATE COMP "CH1_DATA3_N"  SITE "AA15" ;
LOCATE COMP "CH2_DCK_P"    SITE "AA7" ;
LOCATE COMP "CH2_DCK_N"    SITE "AB7" ;
LOCATE COMP "CH2_DATA0_P"  SITE "AA6" ;
LOCATE COMP "CH2_DATA0_N"  SITE "AB6" ;
```

```
// XO3D CrossLink Connections Continued
LOCATE COMP "CH2_DATA1_P"  SITE "AA9" ;
LOCATE COMP "CH2_DATA1_N"  SITE "AB9" ;
LOCATE COMP "CH3_DCK_P"    SITE "AB19" ;
LOCATE COMP "CH3_DCK_N"    SITE "AA19" ;
LOCATE COMP "CH3_DATA0_P"  SITE "AB18" ;
LOCATE COMP "CH3_DATA0_N"  SITE "AA18" ;
LOCATE COMP "CH3_DATA1_P"  SITE "AB20" ;
LOCATE COMP "CH3_DATA1_N"  SITE "AA20" ;
LOCATE COMP "SDA1"    SITE "AA11" ;
LOCATE COMP "SCL1"    SITE "AB11" ;
LOCATE COMP "SDA2"    SITE "AB13" ;
LOCATE COMP "SCL2"    SITE "AA13" ;
LOCATE COMP "FX_SN"      SITE "AA3" ;
LOCATE COMP "FX_SCLK"    SITE "T9" ;
LOCATE COMP "FX_MOSI"    SITE "AA21" ;
LOCATE COMP "FX_MISO"    SITE "U9" ;
LOCATE COMP "RESETN"     SITE "AB3" ;
```

References

For more information, refer to the following documents:

- L-ASC10 In-System Programmable Hardware Management Expander Data Sheet (FPGA-DS-02038)
- MachXO3D Programming and Configuration Usage Guide (FPGA-TN-02069)
- Programming Cable User Guide (FPGA-UG-02042)
- MachXO3D Slew Rate Control Demo User Guide (FPGA-UG-02067)
- MachXO3D Dual Boot Demo User Guide (FPGA-UG-02068)
- MachXO3D Hitless I/O and Hitless EBR Demo User Guide (FPGA-UG-02069)

Revision History

Revision 1.0, May 2020

Section	Change Summary
All	Initial release.

www.latticesemi.com